

Agilent E2976A System Validation Package 2.1

User's Guide



Agilent Technologies

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Author: Anja Schauer, t3 medien GmbH

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Contents

Introduction	7
Theory of Operation	7
Data Paths Overview	9
Test Coverage	10
PPR, the Key Technology	11
Getting Started	13
Test Example	14
Preparing for Setting Up the Test Example	17
Setting Up the Example Test Configuration	19
Defining Test Functions	21
Setting Testcard Properties	26
How to Set Properties	27
PCI-X Testcard Settings	29
Running the Test Example	31
Analyzing the Test Report	32
The Test Configurations	37
Possible Hardware Configurations	37
Testcard Control	38
The Front Side Interface Executable	39
Identification of Card Numbers	40

The Available Tests	43
General Test Description	43
Standard Tests	45
Busload Generator	45
Testcard to System Memory	46
CPU to Testcard	46
CPU and Testcard to System Memory	47
Peer-To-Peer Traffic	48
Master-To-Target Traffic	49
Testcard Read from System Memory	50
Protocol Checker	50
PCI Configuration Scan	50
Testcard to System Memory - User Address	51
PCISIG Compliance Tests	51
MLT - Master Latency Test	51
SIG Post Test	52
SIG Interrupt Routing Test	53
CPU to Testcard Address and Testcard to System Memory	54
Address	54
SIG Card Test	55
PMTEST - Power Management Test	55
TYPE1 - Type 1 Test	56
DISCARD - Discard Test	56
MCT Test - Maximum Completion Time Test	56
Recommendations on Test Duration	57
Testing with the User Interface	59
Testing Principles	60
Setting Up the Test Configuration	62
Defining Test Functions	63
Check Testcard Settings	66
Running the Test	69

Test Results	71
Log File Description	72
Report File Description	73
Error Handling	74
Setup File Reference	77
Settings File Formats	78
Scenario and Test Parameter	79
Testcard Parameters	80
Testcard and Location Information	80
Card Features Settings	81
Master Settings (for PCI Testcards)	82
Target Settings (for PCI Testcards)	84
Requester Settings (for PCI-X Testcards)	85
Completer Settings (for PCI-X Testcards)	86
Protocol Checker (Rule Masking)	87

Introduction

This section introduces the E2976A System Validation Package (SVP). It gives an idea of the general use of this software tool and shows how it is best included in your test environment. This section also gives an overview of the different data paths that can be tested in your PCI/PCI-X system and the types of tests that can be made with this tool.

Theory of Operation

The E2976A System Validation Package is a ready-to-use software package that performs system stress tests during the validation phase PCI- or PCI-X based systems. The tool sets up and controls several Agilent PCI and PCI-X testcards to create application-realistic system traffic. This allows you to set up fully predictable traffic scenarios and provides measurable test coverage and test repeatability.

With the System Validation Package, the system validation process is significantly enhanced by:

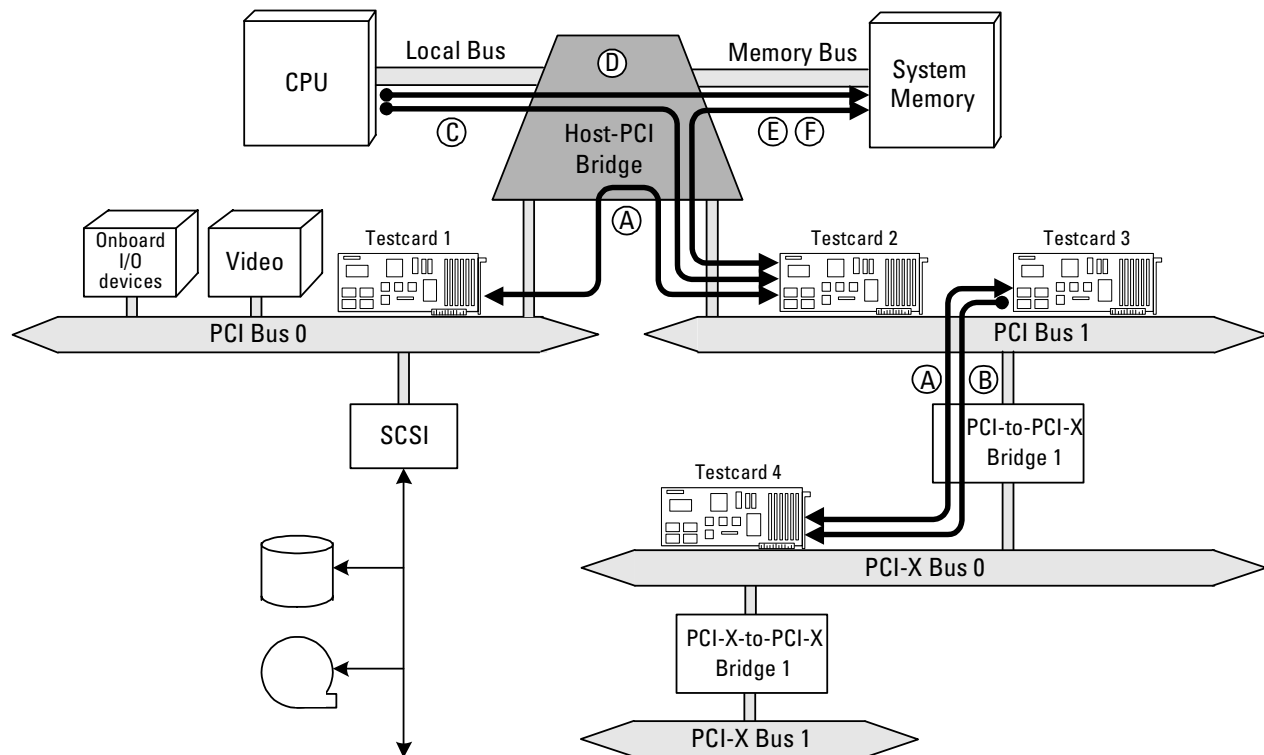
- Putting the data paths in I/O systems under stress in a controlled and predictable way.
- Running several tests in parallel to increase system stress on multiple data paths.
- Independence of test and software architecture from the I/O system (PCI, PCI-X, System I/O).
- Providing the ability to control multiple testcards for different I/O systems (PCI 1x/2x/4x, PCI-X).
- Internal testcard controlling (controlling host on SUT), or external controlling, using a separate host computer (RS-232, Parallel/Fast Host, USB connection).

- Allowing full configuration; settings can be stored to and retrieved from disk.
- Providing extensive static reports (settings and configuration) and live reports (test progress and results).
- Providing ready-to-run tests to force the most critical conditions for the system.
- Providing a series of tests defined by the PCI Special Interest Group (PCISIG) that can be used to verify that devices and systems are compliant to the PCI and PCI-X specification.
- Providing repeatable tests for failure analysis and failure regression tasks.
- Supporting comparison of test results for performance evaluation and further system improvements.
- Making an easy link to R&D's debug environment.

Data Paths Overview

The Agilent PCI and PCI-X testcards can be plugged into any PCI/PCI-X bus of the system under test. This allows the testing of a variety of data paths. The System Validation Package provides a whole range of test actions for testing the different data paths. The letters in parentheses in the following list correspond to the data paths indicated in the figure below.

- Peer-to-peer traffic between two testcards (A)
- Master-to-target traffic between two testcards (B)
- CPU to testcard (C)
- CPU and testcard to system memory (D and E)
- Testcard to system memory (E)
- Testcard to system memory – User Address (E)
- Testcard read from system memory (F)



Additionally, the System Validation Package provides the Protocol Checker test and the PCI or PCI-X Configuration Scan test, which passively observe devices on the PCI or PCI-X bus.

The System Validation Package also provides several PCISIG tests.

Test Coverage

Two of the main problems of typical test methods for system validation are that they take a long time and are difficult to repeat. The usual approach is to simply plug standard PCI and PCI-X testcards into the system under test, load them with traffic and wait until an error occurs. Even with very long tests, there is a high probability that not all possible scenarios will be tested.

The advantage of the System Validation Package is that you can design tests specifically for certain system-critical conditions. These tests can then be repeated as necessary. Furthermore, you can also let the SVP go through all possible variations of parameters, such as commands and block sizes, so that all situations that the system may face are covered.

Thus, you can cover all traffic situations for the system to be tested within minutes. The technology providing this coverage is called the PPR technology.

PPR, the Key Technology

The Agilent Protocol Permutator & Randomizer (PPR) technology allows you to overcome the lack of repeatable test conditions with very high and predictable test coverage.

PPR permutes the PCI or PCI-X protocol parameters and data traffic in a pseudo-random way. More specifically, all memory accesses are varied through all possible combinations of their attributes. This applies for varying block sizes and the use of the different memory commands, such as write, read, write invalidate, read line, and read multiple. Furthermore, permutations are made in terms of the alignments and byte enables. This means that all variations of byte, word, and dword accesses are used.

Permutations also include protocol attributes, which ensures that the transactions are performed with

- all possible wait states inserted by both the Exerciser's master and target,
- all possible transaction terminations by the target (except for target abort),
- both 64-bit and 32-bit accesses attempted by the master,
- both acceptance and non-acceptance of 64-bit accesses by the target.

Thus, not only critical test patterns can be transferred between different system components, they are also automatically permuted to emulate all thinkable traffic scenarios.

For more information on how the Protocol Permutator & Randomizer works, please refer to the *Agilent C-API/PPR Programmer's Guide*, which is delivered with the testcard.

Getting Started

To set up a system test with the Agilent E2976A SVP Graphical User Interface (GUI), several steps are needed. This guided tour shows these steps by means of an example.

The recommended approach is:

1. Test preparation
Insert testcards and start the software.
2. Test configuration
Define the scenarios.
3. Definition of test functions
Set test parameters and select testcards for each test.
4. Definition of testcard properties
Check and modify master, target and protocol checker settings.
5. Test execution
Run the test and get the test report.

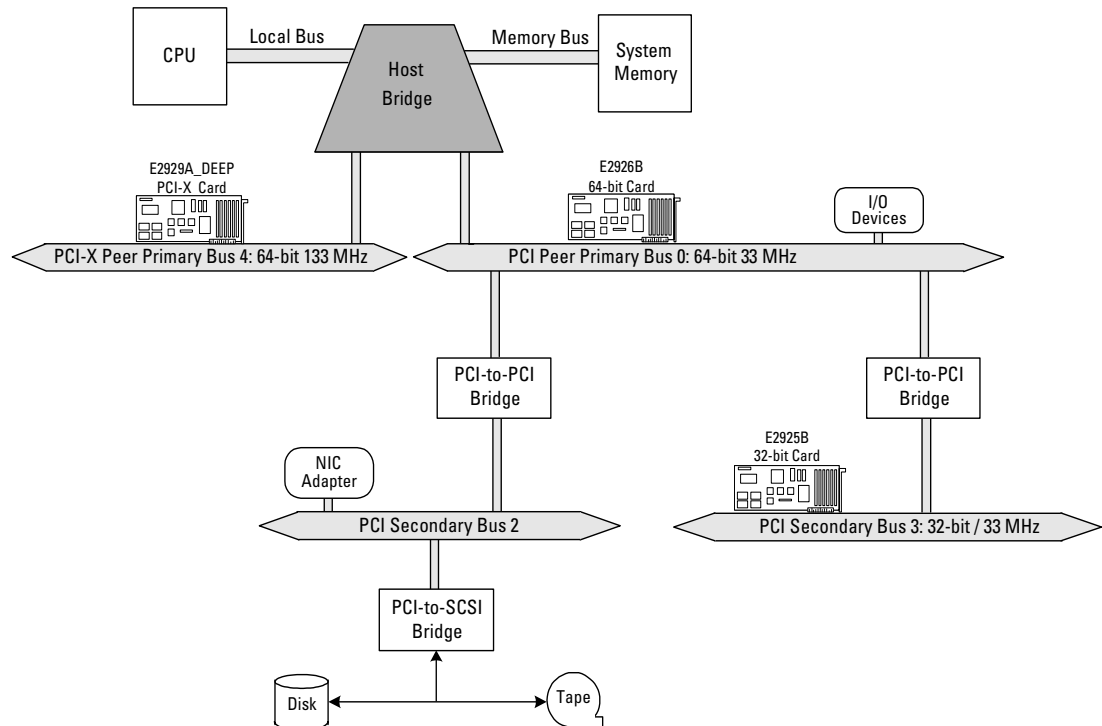
In this guided tour, you are shown how to set up a system test by means of a possible test configuration and some selected tests that are provided with the Agilent E2976A SVP software. These tests perform configuration space scanning, CPU interaction and stressing one PCI-to-PCI bridge, for example.

The online mode is used as a basis. If it is not possible for you to insert the required testcards, you can set up a system test in offline mode, but you cannot execute it. Reference is made to the differences between online and offline mode.

The test example is also available as a VPS file, which is delivered with the Agilent E2976A software. To view this example, switch to offline mode and open `guided_tour.vps`.

Test Example

Task A new system has been configured using a PCI-X bus, several PCI busses, PCI-to-PCI bridges and other devices. The system looks like this:



The task is to check the overall system stability, focussing especially on the data path between Bus 0 and Bus 3 (the PCI-to-PCI bridge) and the data paths to the system memory. These data paths are stressed to detect protocol errors and data errors.

Solution Predefined tests provided by the Agilent E2976A SVP software will be used for:

- transferring data from the CPU to a testcard
- accessing the system memory from a testcard
- generating traffic in both directions between two testcards
- generating additional bus load for one bus
- scanning the configuration space of the bus system

These tests require three testcards inserted into the system under test as shown in the picture above.

Implementation To use these features, three scenarios must be set up. The scenarios will be executed one after the other, the tests within each scenario will be executed concurrently.

- Scenario 1

This scenario includes two tests that run concurrently. To check and report the system configuration, the configuration space of both the PCI-X bus and the PCI bus are scanned by using the Configuration Scan test. To set up this test, the following settings are used:

Test Function to be used:	configscan	configscan
Testcard to be used:	E2929A_DEEP (Bus 4)	E2926B (Bus 0)
Duration of the tests:	60 seconds	60 seconds
Start Delay:	0	0
Bandwidth:	100 %	100 %

The test tries to occupy the bus with the whole bus bandwidth of 64 bit. This target bandwidth cannot always be achieved.

- Scenario 2

This scenario includes two tests that run concurrently. The CPU to Testcard test transfers data from the CPU to a testcard on Bus 0. The Testcard to System Memory test accesses the system memory from a testcard on Bus 3. The following settings are used:

Test Functions to be used:	cpu2card	cardtosystemmem
Testcards to be used:	E2926B (Bus 0)	E2925B (Bus 3)
Duration of the tests:	75 seconds	75 seconds
Start Delay:	0	0
Bandwidth:	100 %	100 %

Both tests try to occupy the whole bandwidth of Bus 0 and Bus 3.

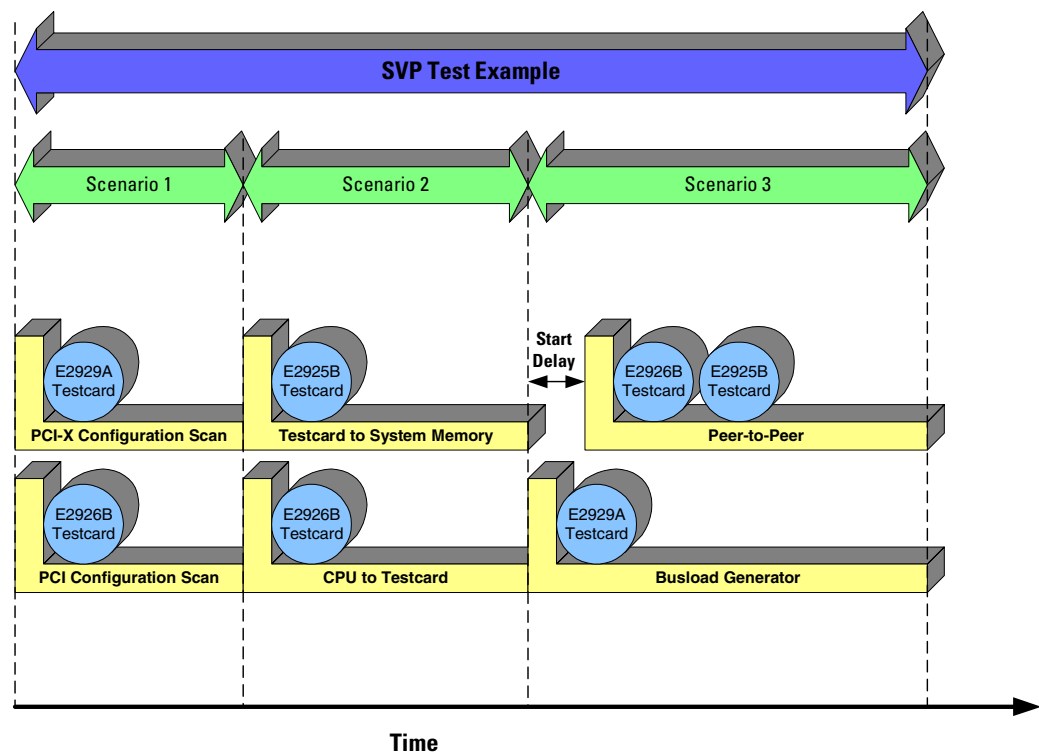
- Scenario 3

This scenario includes two tests that run concurrently. The Peer-to-Peer test generates traffic between testcards on Bus 0 and Bus 3 in both directions. The bus load test generates additional load on PCI-X Bus 4. The following settings are used:

Test Functions to be used:	peer2peer	busload
Testcards to be used:	E2926B (Bus 0), E2925B (Bus 3)	E2929A_DEEP (Bus 4)
Duration of the tests:	200 seconds	215 seconds
Start Delay:	15 seconds	0 seconds
Bandwidth:	100 %	100 %

The SVP software allows you to delay the start of a test and to use tests with different durations.

Timing The following figure shows the whole test configuration and the timing.



Preparing for Setting Up the Test Example

To prepare for the test example:

- 1 Before you use the software, consider which busses in your system under test are to be checked. You need to insert at least one testcard per tested bus.

- 2 Start the Agilent E2976A System Validation Package software.

For this test, we assume that the software is running on the system under test.


The software is in online mode by default and automatically scans the testcards connected to the system under test.

All available testcards are listed in the *Cards Available* list in the SVP object window which is always visible when you start the software.

By default, the testcards are named with Testcard 1, Testcard 2 and Testcard 3.

Test Setup in Offline Mode

If your system differs from that shown in the test example and if it is not possible for you to insert the required testcards, you can set up the test example in offline mode. To set up tests in offline mode:

- 1 Switch the software to the offline mode by clicking the icon  in the tool bar.

You can now define the testcards by inserting testcards into the *Available Cards* item in the navigator.

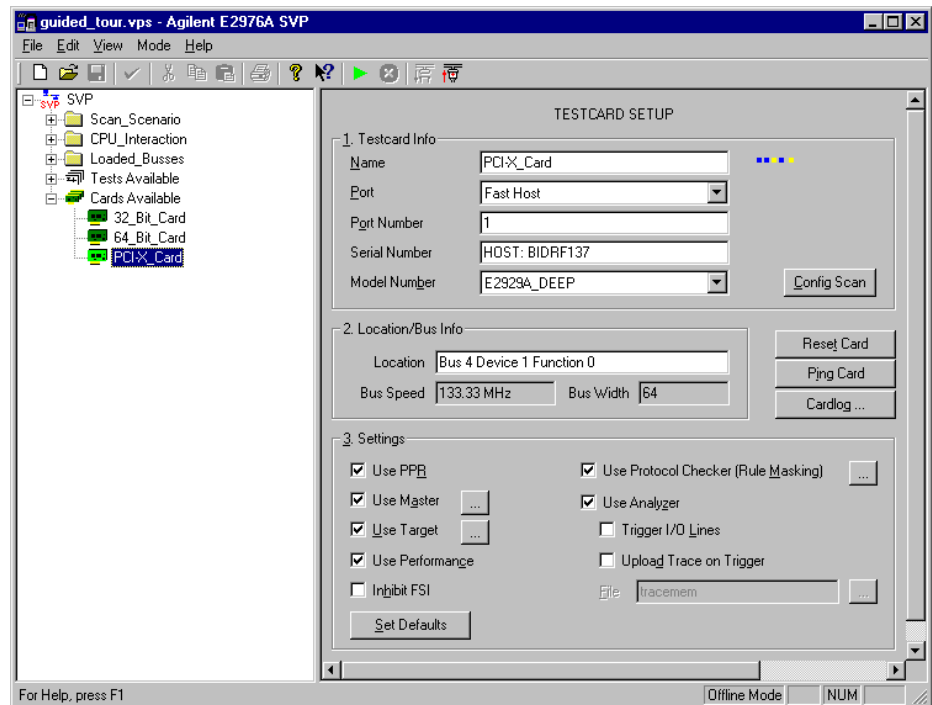
- 2 Click the *Available Cards* item and select *Insert New Card* from the *Edit* menu.

This inserts a new testcard in the navigator.

- 3 Repeat step 2 as necessary.

Renaming Testcards To rename the testcards:

- 1 Click the Testcard 1 item in the navigator and enter **32_Bit_Card** in the *Name* field in the Testcard Setup window.
- 2 Rename Testcard 2 to **64_Bit_Card** and Testcard 3 to **PCI-X_Card** in the same way.



Setting Up the Example Test Configuration

The Agilent E2976A SVP software provides one scenario by default. For the test example, you need to insert another two scenarios and assign the test functions to the scenarios.

Create the Scenarios

To create all scenarios:

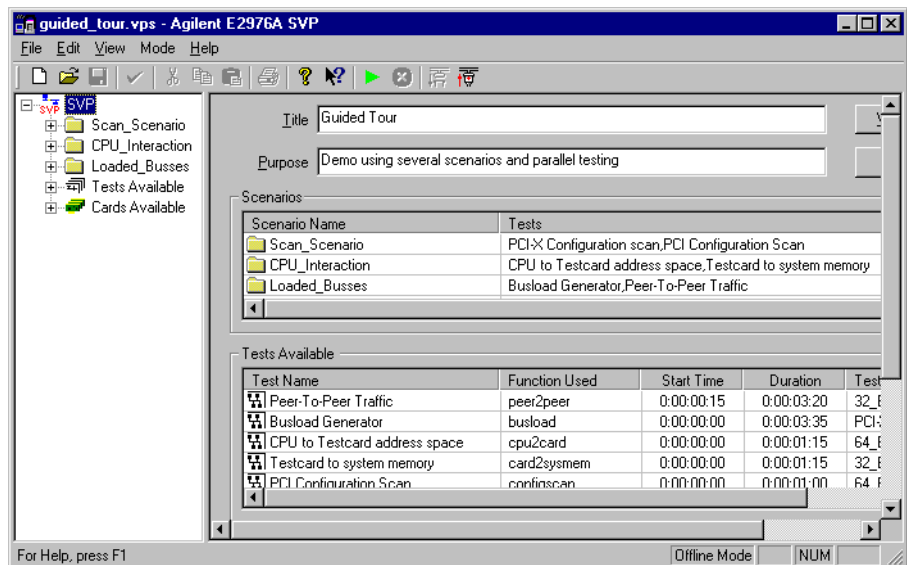
- 1 Click the SVP object in the navigator and select *Insert New Scenario* in the *Edit* menu.

This inserts one scenario into the navigator.

- 2 Repeat step 1 for the third scenario.

- 3 Click the Scenario_1 item in the navigator and enter the new name **Scan_Scenario** in the *Name* field in the Scenario Details window. The new name will appear in the navigator.

- 4 Rename Scenario_2 and Scenario_3 to **CPU_Interaction** and **Loaded_Busses**.

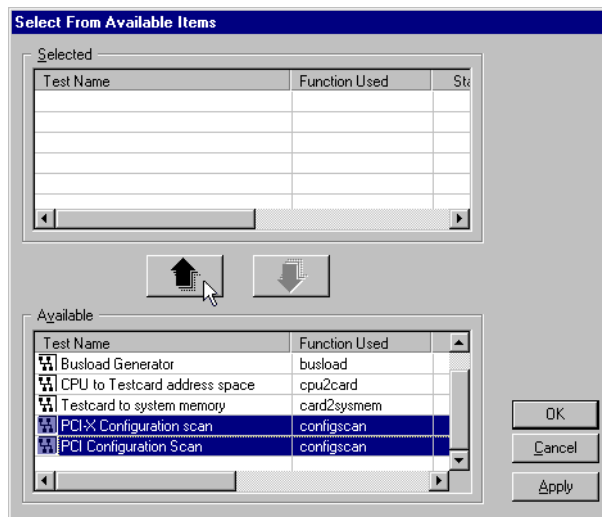


Insert Tests in Scenarios To insert the PCI-X Configuration scan test in the Scan_Scenario scenario:

- 1 Click the Scan_Scenario in the navigator and click the *Select Test(s)* button in the Scenario Details window.

This opens the *Select From Available Items* dialog box.

- 2 Select the *PCI-X Configuration scan* test and the *PCI-X Configuration scan* from the *Available* drop-down list and click the distribution arrow.



Both the PCI-X Configuration scan test and the PCI Configuration scan test will then appear in the *Selected* list.

- 3 Repeat steps 1 and 2 to insert
 - the CPU to Testcard test and
 - the Testcard to System Memory test
 into the CPU_Interaction scenario.
- 4 Repeat steps 1 and 2 to insert
 - the Busload Generator test and
 - the Peer-to-Peer Traffic test
 into the Loaded_Busses scenario.

NOTE It is possible to insert new tests in the *Available* list and remove available tests from the *Available* list. For further information, see “*Defining Test Functions*” on page 63.

Defining Test Functions

In the previous section, several test functions have been merged into different scenarios. The Agilent E2976A SVP software provides default settings for these tests. For our task, some test settings are to be modified. How this takes place is shown in this section.

Because the main steps are the same for all tests, only the setup for the PCI-X Configuration Scan test is described in all details.

PCI-X Configuration Scan Test Setup

To set up the PCI-X configuration scan test:

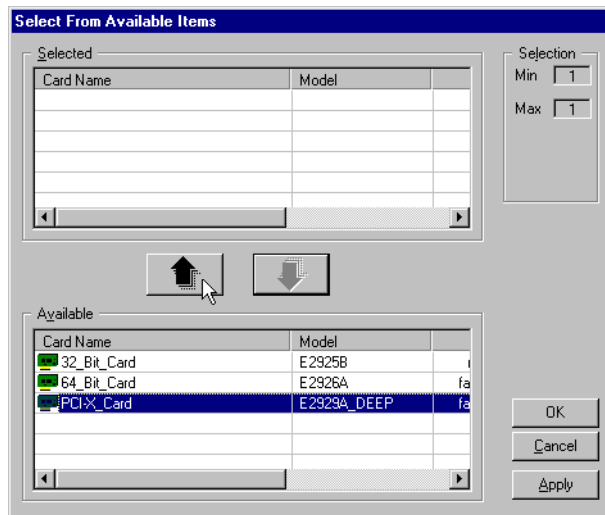
- 1 Click the PCI-X Configuration scan test in the navigator to open the respective Test Setup window.

The default parameter settings can be used in this PCI-X configuration scan test.

- 2 Click the *Select Card(s)* button.

This opens the *Select From Available Items* dialog box.

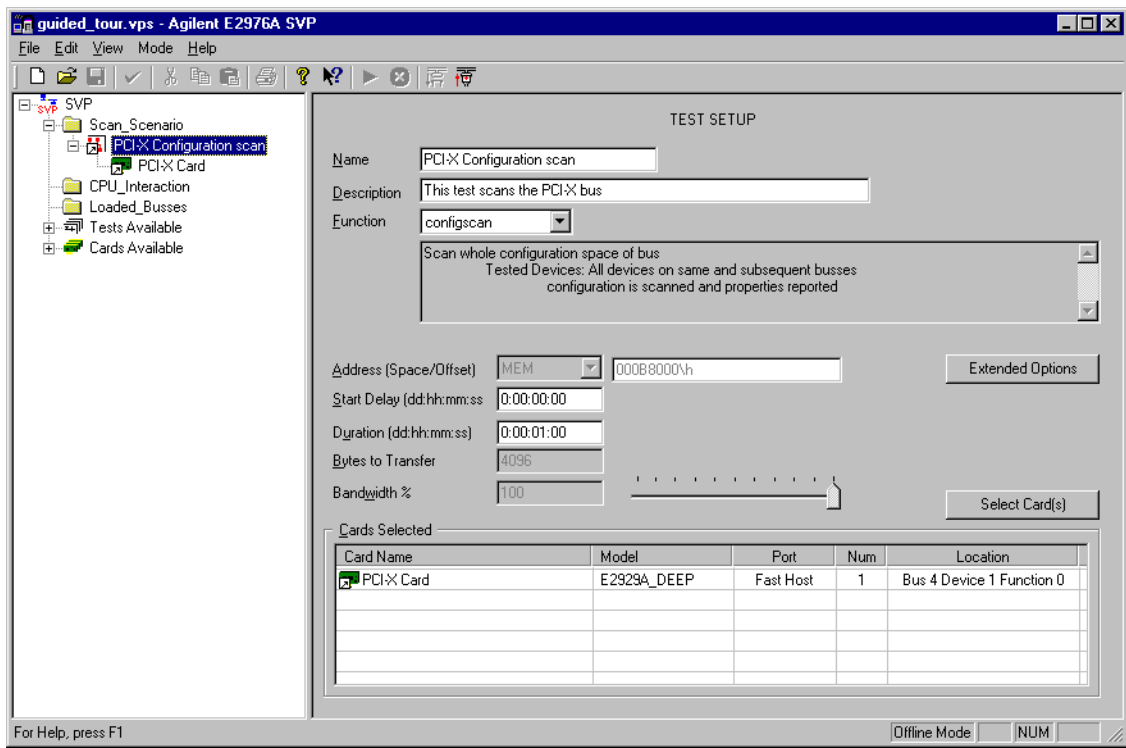
- 3 Select from the *Available* list the *PCI-X_Card* testcard and click the distribution arrow.



The *PCI-X_Card* testcard will then appear in the *Selected* list.

- 4 Click *OK* to close the dialog box.

The resulting Test Setup window is:



You can get a short description of the current test below the *Function* drop down list.

PCI Configuration Scan Test To set up the PCI configuration scan test:

- 1 Open the Test Setup window for the PCI Configuration scan test.
The default parameter settings can be used in this test.
- 2 Select the *64_Bit_Card* testcard for this test.

CPU to Testcard Test Setup To set up the CPU to Testcard test:

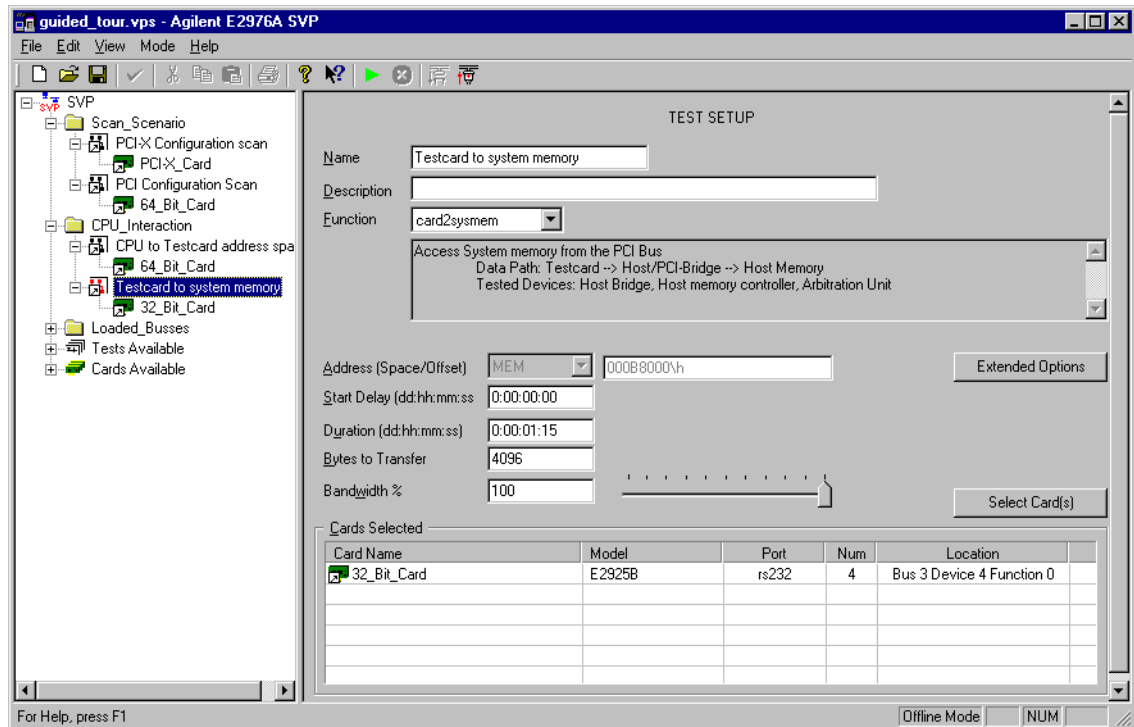
- 1 Open the Test Setup window for the CPU to Testcard Address Space test.
The testcard memory address space (*MEM*) is selected by default.
- 2 Enter a value of **1** minutes and **15** seconds in the *Duration* field.
- 3 Select the *64_Bit_Card* testcard for this test.

Testcard to System Memory Test Setup

To set up the Testcard to System Memory test:

- 1 Open the respective Test Setup window for the Testcard to System Memory test.
- 2 Enter a value of **1:15** seconds in the *Duration* field.
- 3 Select the *32_Bit_Card* testcard for this test.

The resulting Test Setup window is:



Busload Generator Test Setup

To set up the Busload Generator test:

- 1 Click the Busload Generator test in the navigator to open the respective Test Setup window.

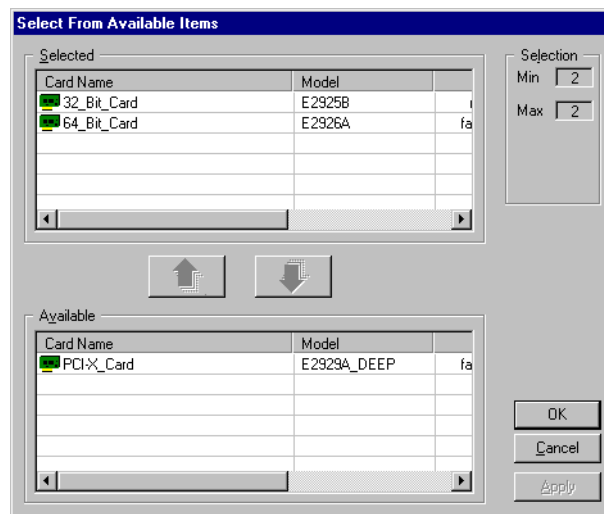
The testcard memory address space (*MEM*) is selected by default.

- 2 Enter a value of **3** minutes and **35** seconds in the *Duration* field.
- 3 Select the *PCI-X_Card* testcard for this test.

Peer-To-Peer Traffic Test Setup To set up the Peer-To-Peer Traffic test:

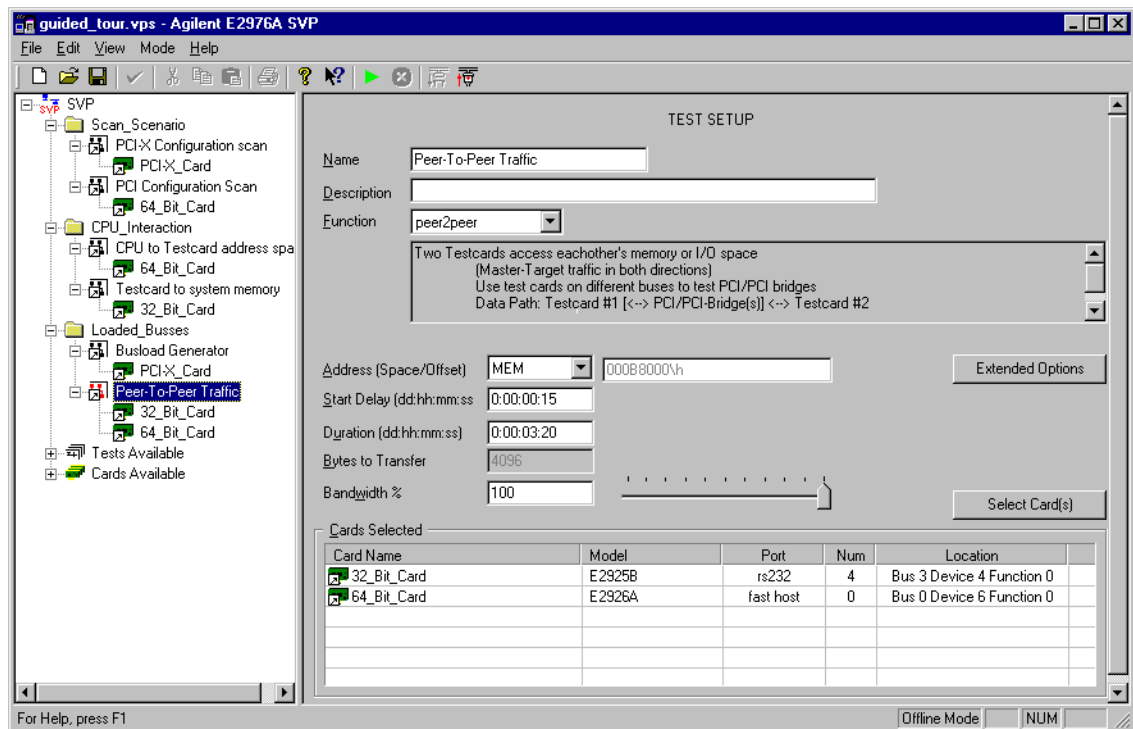
- 1 Open the Test Setup window for the Peer-To-Peer Traffic test.
- 2 Enter a value of 15 seconds in the *Start Delay* field.
- 3 Enter a value of 3 minutes and 20 seconds in the *Duration* field.
- 4 Select the *32_Bit_Card* testcard and the *64_Bit_Card* testcard for this test.

The resulting Select From Available Items dialog box is:



For this test, two testcards are required. The SVP software prevents the selection of more or less testcards. The limits are shown under *Selection*.

The resulting Test Setup window is:



Setting Testcard Properties

The Agilent E2976A SVP software provides testcard settings for all available testcards by default. The settings are available via the Testcard Setup window and can be adapted to the actual tests.

The settings determine which testcard features are active. If the master, target, PPR and protocol checker features are active, you can select further testcard properties, for example, various read/write commands. These properties are available via the details buttons next to the respective check boxes.

NOTE The available testcard properties differ between PCI and PCI-X testcards.

In the test example, the identical master and target settings for all PCI testcards are used.

As an example, it is shown how the properties of the 32_Bit_Card testcard are set. Furthermore, the settings for the PCI-X testcard are shown.

How to Set Properties

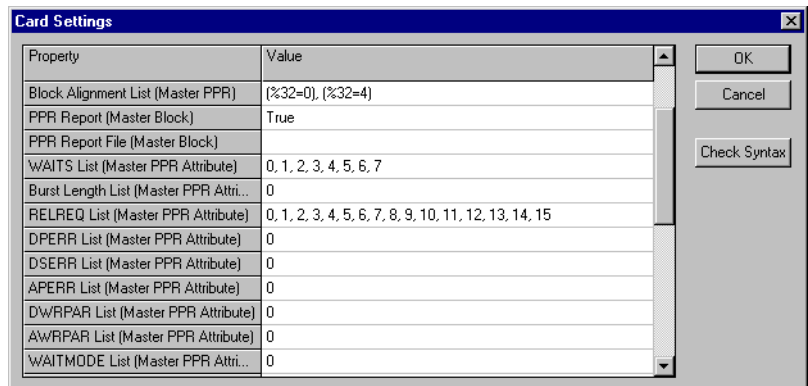
To set master, target and protocol checker properties of the 32_Bit_Card testcard:

- 1 Open *Cards Available* in the navigator and select the 32_Bit_Card testcard.

This opens the Testcard Setup window of this testcard.

- 2 Click the details button next to the *Use Master* check box.

This opens the master *Card Settings* dialog box.



- 3 For the example the following master properties can be set:

Property	Value	Description
PPR Report File (Master Block)	mblock.rpt	File name for the master block report.
WAITMODE List (Master PPR Attribute)	0, 1	List of values to keep the address constant during the WAITMODE phases or not: 0: Address is stable 1: Address toggles
STEPMODE List (Master PPR Attribute)	0, 1	List of values to keep the address constant during the STEPS phases or not: 0: Address is stable 1: Address toggles
TRYBACK List (Master PPR Attribute)	0, 1	List of Fast Back-to-Back cycle tries: 0: Does not try Fast Back-to-Back cycle. 1: Tries Fast Back-to-Back cycle.
DELAY List (Master PPR Attribute)	0	No master transaction delay.

- 4 Click OK to verify the settings.

- 5 Click the details button next to the *Use Target* check box.

This opens the target *Card Settings* dialog box.

Property	Value
TERM List (Target PPR Attribute)	32*noterm, 2*retry, disconnect
WAITS List (Target PPR Attribute)	1, 2, 3, 4, 5, 6, 7, 8
DPERR List (Target PPR Attribute)	0
DSERR List (Target PPR Attribute)	0
APERR List (Target PPR Attribute)	0
WRPAR List (Target PPR Attribute)	0
ACK64 List (Target PPR Attribute)	0, 1
DACPERR List (Target PPR Attribute)	0
WRPAR64 List (Target PPR Attribute)	0
PPR Report (Target Attribute)	True
PPR Report File (Target Attribute)	

Buttons: OK, Cancel, Check Syntax

- 6 For the example the following target properties can be set:

Property	Value	Description
Termination List (Target PPR Attribute)	0	No termination.
Waits List (Target PPR Attribute)	0, 1, 2, 3, 4, 5, 6, 7, 8	List of number of waits that are permuted.
PPR Report File (Target Attribute)	tattr.rpt	File name for the target attribute report.

- 7 Click OK to verify the settings.

- 8 Click the details button next to the *Use Protocol Checker (Rule Masking)* check box.

This opens the Protocol Rule Masking dialog box.

Index	Rule	State
31	SEM 1	Enabled
32	SEM 3	Enabled
33	SEM 5	Enabled
34	SEM 6	Enabled
35	SEM 7	Enabled
36	SEM 8	Enabled
37	SEM 9	Enabled
38	SEM 12	Enabled
39	SEM 13	Enabled
40	LAT 0	Enabled

Buttons: Enable All, Disable All, OK, Cancel

Mask Rule(s) After x Occurrences: 3

- 9 Disable SEM8, SEM9 and LAT0 by clicking into the state column of the specified rules.

Violations of these rules will not be detected.

- 10 Click OK to verify the settings.

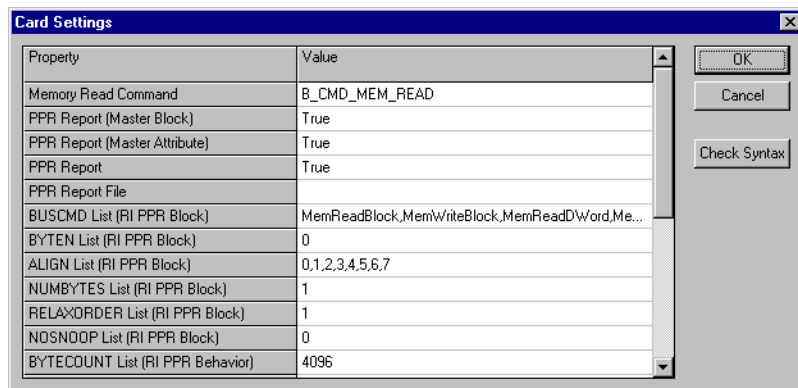
PCI-X Testcard Settings

Setting requester, completer and protocol checker properties of the PCI-X_Card testcard takes place in the same way as described for the 32_Bit_Card testcard.

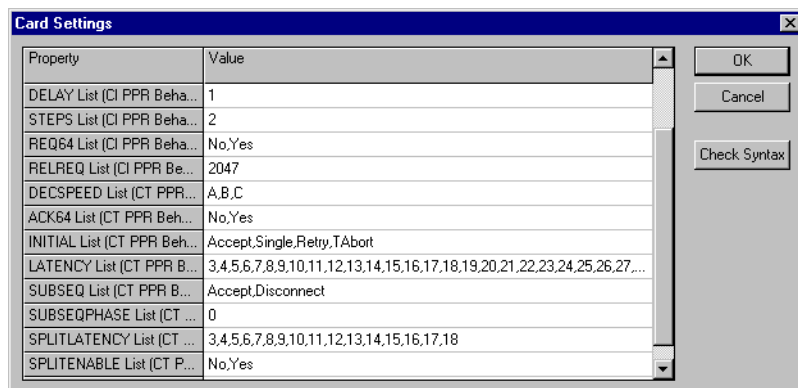
NOTE To open the respective Card Settings dialog boxes for PCI-X testcards, the details buttons of *Use Master*, *Use Target* and *Use Protocol Checker (Rule Masking)* must be clicked.

This section only shows the Card Settings dialog boxes and the settings used in this guided tour example.

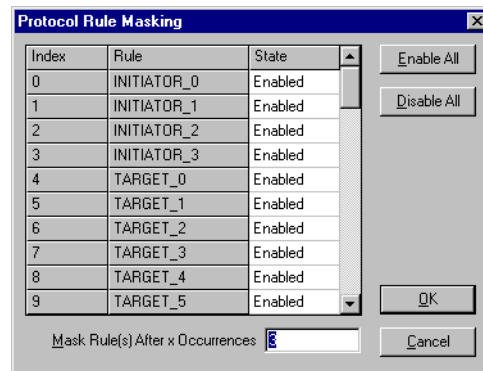
Requester Card Settings For the requester card properties of the *PCI-X_Card* testcard, the default settings are used. The requester *Card Settings* dialog box for PCI-X testcard looks as follows.



Completer Card Settings For the target properties of the *PCI-X_Card* testcard, the default settings are used. The target *Card Settings* dialog box for PCI-X testcard looks as follows.



Protocol Rule Masking For the protocol checker properties of the *PCI-X_Card* testcard, the default settings (all rules are enabled) are used. The Protocol Rule Masking dialog box looks as follows.





Running the Test Example

NOTE You can only run the test if all testcards are available.

To run the test example:

- 1 Ensure that you are in online mode.

If not, click the go online icon  in the toolbar.

- 2 Click the run icon  in the toolbar.

The software automatically opens the *SVP Reporting* dialog box where the test report is shown.

The resulting test report is displayed in the following section. Because new test status information is added to this report every few seconds, the report can be very large. Hence, only a part of the report can be shown here.

Analyzing the Test Report

Report Start The report starts with the start date and time of the test session. The first scenario (Scan_Scenario) with start date and time and its tests (PCI-X Configuration scan and PCI Configuration scan) then follows.

The report shows the initialization, start date and time and the used testcards of the PCI-X Configuration scan test and the PCI Configuration scan test.

```
***** Starting SVP Testing at 12-Dec-2000, 14:00:42 h *****
----- Scenario <Scan_Scenario> -----
+++++++ Scenario <Scan_Scenario> ++++++

***** Starting scenario at 12-Dec-2000, 14:00:49 h
Starting Scenario <Scan_Scenario> at 12-Dec-2000, 14:00:49 h

----- Test <PCI-X Configuration scan> -----
Initializing test PCI-X Configuration scan with function PCI
Configuration scan
Starting Test <PCI-X Configuration scan> at 12-Dec-2000, 14:00:49 h
----- Testcard <PCI-X_Card> -----
Starting Testcard <PCI-X_Card> at

----- Test <PCI Configuration Scan> -----
Initializing test PCI Configuration Scan with function PCI Configuration
scan
Starting Test <PCI Configuration Scan> at 12-Dec-2000, 14:00:49 h

----- Testcard <64_Bit_Card> -----
Starting Testcard <64_Bit_Card> at 12-Dec-2000, 14:00:49 h
```


Scenario Initialization For each scenario, the expired time of the tests and the status of the testcards used in the tests are listed.

The third scenario (Loaded_Busses) is used as an example. The report shows the start time of the scenario and the initialization of the Busload Generator and the Peer-to-Peer Traffic test.

Furthermore, start date and time of the Busload Generator test and the status of the PCI-X_Card testcard are shown.

```

+++++++ Scenario <Loaded_Busses> ++++++

***** Starting scenario at 12-Dec-2000, 14:04:13 h
Starting Scenario <Loaded_Busses> at 12-Dec-2000, 14:04:13 h

----- Test <Busload Generator> -----
Initializing test Busload Generator with function Busload Generator
Setting up card PCI-X_Card with address <MEM:00000001 00100000\h> for
Busload Generator
----- Test <Peer-To-Peer Traffic> -----
Initializing test Peer-To-Peer Traffic with function Peer-To-Peer Traffic
Setting up card 32_Bit_Card with address <MEM:FED00000\h> for Peer-To-Peer
Traffic
Setting up card 64_Bit_Card with address <MEM:FBE00000\h> for Peer-To-Peer
Traffic

----- Scenario <Loaded_Busses> -----
time into scenario is 2 s.

***** Report at 12-Dec-2000, 14:04:15 h

----- Test <Busload Generator> -----
Starting Test <Busload Generator> at 12-Dec-2000, 14:04:14 h
time into test is 1 s.

----- Testcard <PCI-X_Card> -----
Starting Testcard <PCI-X_Card> at 12-Dec-2000, 14:04:14 h
Performance Status
  whole bus: Utilization  91.77% / Throughput  60.42% / Efficiency  65.84%
  this card: Utilization  91.77% / Throughput  60.42% / Efficiency  65.84%
----- Test <Peer-To-Peer Traffic> -----
Test ready, waiting for start delay (15 s) to expire

```

Test Results During test execution, the status of the trace memory trigger and the observer is shown.

In defined intervals (3 seconds), the performance of the whole bus and testcards used in this actual scenario and all errors that can be found with a testcard are displayed. The observer status gives information about the first occurring protocol errors and the accumulating subsequent errors.

The detected protocol errors are listed by specifying the violated protocol rule. A short description is also provided.

```

----- Test <Busload Generator> -----
time into test is 19 s.

----- Testcard <PCI-X_Card> -----
Performance Status
  whole bus: Utilization  99.05% / Throughput  65.22% / Efficiency  65.84%
  this card: Utilization  99.05% / Throughput  65.22% / Efficiency  65.84%

----- Test <Peer-To-Peer Traffic> -----
time into test is 0 µs.

----- Testcard <32_Bit_Card> -----
Performance Status
  whole bus: Utilization  95.47% / Throughput  20.36% / Efficiency  21.33%
  this card: Utilization  95.47% / Throughput  20.36% / Efficiency  21.33%
Tracememory trigger occurred
Observer Status:
  PROTOCOL ERROR:
  49: SEM 6:An INTx signal has been asserted and deasserted before an
  Interrupt Acknowledge cycle occurred.
  ACCUMULATED PROTOCOL ERRORS:

----- Testcard <64_Bit_Card> -----
Starting Testcard <64_Bit_Card> at 12-Dec-2000, 14:04:33 h
Performance Status
  whole bus: Utilization  94.11% / Throughput  20.42% / Efficiency  21.70%
  this card: Utilization  92.83% / Throughput  20.32% / Efficiency  21.89%
Tracememory trigger occurred

```

Final Report Each scenario report ends with a final report. This report contains the test results (maximum performance for the whole bus and the used testcard) and the protocol checker results. That means, the number of rule violations per rule and testcard and the number of occurred errors in this scenario are listed.

After the final report, the total elapsed time of the scenario is shown.

```

+++++++ Scenario <Loaded_Busses> ++++++

***** Final Report at 12-Dec-2000, 14:07:56 h

----- Testcard <PCI-X_Card> -----
Test results:
  Maximum Performance during test:
    whole bus: Utilization 99.05% / Throughput 65.22% / Efficiency 65.84%
    this card: Utilization 99.05% / Throughput 65.22% / Efficiency 65.84%
Protocol checker results:
  No violations found.
Data compare unit results:
  No errors.

----- Testcard <32_Bit_Card> -----
Test results:
  Maximum Performance during test:
    whole bus: Utilization 95.59% / Throughput 20.50% / Efficiency 21.45%
    this card: Utilization 95.59% / Throughput 20.50% / Efficiency 21.45%
Protocol checker results:
  49: violated 3 times, rule has been masked.
  Protocol checker counted total 3 violations
Data compare unit results:
  No errors.

----- Testcard <64_Bit_Card> -----
Test results:
  Maximum Performance during test:
    whole bus: Utilization 94.51% / Throughput 20.70% / Efficiency 21.96%
    this card: Utilization 93.24% / Throughput 20.60% / Efficiency
22.12%
Protocol checker results:
  No violations found.
Data compare unit results:
  No errors.

Scenario finished, 3 errors found.

+++++++ End of final report ++++++
Total elapsed time of Scenario is 3.7167 min.

```

SVP Testing Results At the end of the report, the results of the entire SVP testing are shown.

```
***** SVP Testing Results: *****  
Found total of 6 test errors during testing (see report above).  
***** SVP Testing finished. *****
```

The Test Configurations

This section covers all information needed to run the E2976A System Validation Package (SVP), including a summary of the possible hardware configurations and some recommendations for these configurations to make best use of the SVP.

Internal and external testcard control are also described in this section.

Possible Hardware Configurations

The Agilent E2976A System Validation Package supports the following Agilent PCI and PCI-X testcards:

- E2925B, E2925B_DEEP
- E2926A, E2926A_DEEP
- E2926B, E2926B_DEEP
- E2927A, E2927A_DEEP
- E2928A, E2928A_DEEP
- E2940A, E2940A_DEEP
- E2929A, E2929A_DEEP
- E2929B, E2929B_DEEP
- E2922A
- E2922B

The precondition for the use of the Agilent E2976A System Validation Package with any of these testcards is that the Exerciser option is enabled (option #300).

Several PCI testcards can be plugged into the same PCI bus to increase traffic from different devices or to test different data paths or devices at the same time. You can also plug several testcards into different busses in the system under test, for example, to test the bridges between these busses. You can plug several testcards on busses into the SUT to test the host bridge and the host bridge configuration.

- Recommended Configuration** For every test configuration, the recommended configuration is to have
- one Agilent E2976A System Validation Package license,
 - one testcard for each bus,
 - one additional PCI testcard for a peer-to-peer test on one PCI bus.

Testcard Control

System validation makes it necessary to control many testcards at a time with one system validation tool. This tool allows two methods of controlling testcards: internal and external control.

Internal Control Internal control of testcards means that the SVP software must run on the system under test (SUT).

External Control External control of testcards means that the SVP software runs on a controlling host, which is connected via standard RS-232, USB or via the Fast Host Interface card, which is delivered with the testcard. External control of testcards is used whenever either the SUT's operating system does not support direct access to the I/O busses, or when the SUT's state is not stable enough to sustain a test software running. For test functions that require extra SUT actions, a Front Side Interface Executable is used. These test functions are:

- CPU to testcard
- Testcard to system memory
- CPU and testcard to system memory
- MLT - Master Latency Test
- SIG Post Test
- SIG Interrupt routing test
- CPU to Testcard address and Testcard to system memory address

The Front Side Interface Executable

The Front Side Interface is used whenever internal control of testcards is not desired or cannot be achieved. Communication to FSI takes place using a defined protocol, which communicates via the testcard's mailboxing interface. The software needed to communicate via the mailboxing interface must be running on the system under test. This stand-alone executable is the Front Side Interface Executable (FSI-E) .

Running the FSI-E The FSI-E is executed on the SUT either from a boot floppy, or directly by clicking the *FSI Executable* in the Windows *Start* menu.

Installation for DOS operating systems After you have installed the Agilent E2976A System Validation Package software, you can find the file `fsidos.exe` in the <Installation Directory>\fsidos directory. This is the DOS-Version of the FSI-Executable. You can copy this file via a floppy disk to the destination DOS operating system.

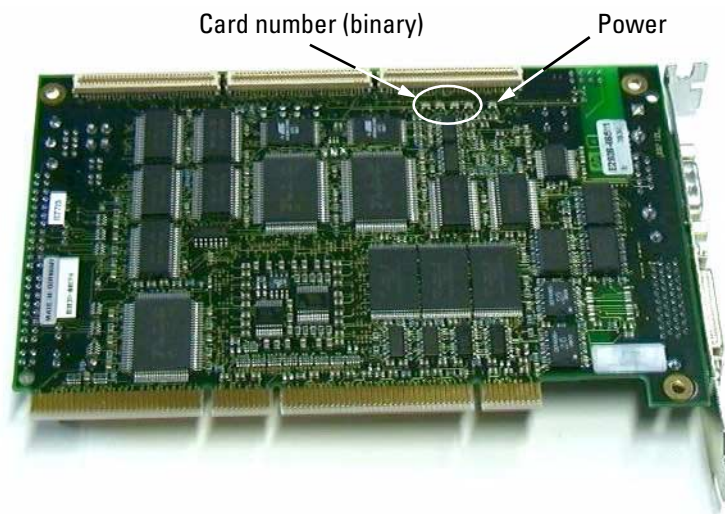
Installation for Windows NT After you have installed the Agilent E2976A System Validation Package software on the destination system, you can start the FSI-E by clicking the *FSI Executable* in the Windows *Start* menu.

Identification of Card Numbers

In case you have several PCI and/or PCI-X testcards plugged into the system under test, the System Validation Package assigns numbers to them in the GUI to tell them apart.

These numbers can be identified on the cards as well:

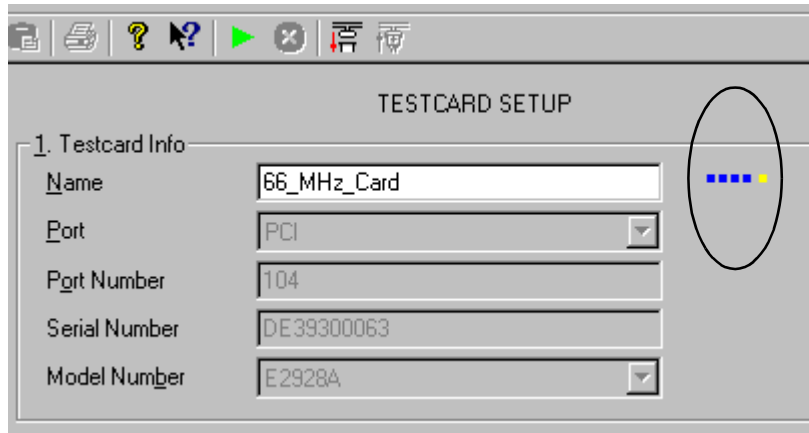
- For PCI testcards, the numbers are coded in a row of five green LEDs along the top edge of the back of the card.



The Power LED at the rear end of the row is separated slightly further than the others. It is always lit when the card is powered and SVP is connected. Closing SVP re-enables heartbeat.

- For PCI-X testcards, the numbers are shown on the numerical LED display at the top edge of the front of the testcard. The numbers are displayed with the format #<three-figure number>, for example, #001.

Card Number LEDs The other four LEDs show a binary coding of the card number, where the LED farthest to the right represents the least significant bit. The pattern of the LEDs is displayed in the GUI next to the card name in the Testcard Setup window for easier identification.



NOTE This applies for all PCI and PCI-X testcards, except the Agilent E2940A CompactPCI testcard. On this testcard, the five LEDs are in a vertical row.

The Available Tests

This section contains information about the different tests that are provided with the E2976A System Validation Package 2.1. It briefly explains how the tests work, which data paths are involved and what requirements must be fulfilled.

General Test Description

Making full use of the testcards' features, the SVP can be used to put data paths within PCI-based computer systems under stress or to test individual chips such as host bridges or PCI-to-PCI bridges. The testcards' analyzer capabilities can be used in parallel to monitor the traffic and to track protocol errors.

Basic Test Structure All tests that use memory accesses to emulate data traffic work with the same structure:

1. Writing a block of data to the destination memory.
2. Reading this data back from the destination memory.
3. Comparing the read data with the initial data field.
4. Writing a block of different data to the same location to make sure that data patterns always change.
5. Reading this data back from the destination memory.
6. Comparing the read data with the data most recently read.
7. Repeating the whole sequence with a different protocol behavior to cover more test cases.
8. Reporting detected errors in data comparison.

Furthermore, you can use cross-triggering with these tests. Cross-triggering means that you connect the trigger I/O ports of two testcards. If a trigger event occurs on one testcard, the other is also triggered. This is very useful, for example, to capture the data traffic on two busses at the same time, because problems on one bus may have their root cause on another bus.

The following table gives an overview of the tests defined in the test library and their requirements.

Test	Number of Cards	Master	Target	Other	Remark
Testcard Read from System Memory	1	X	System main memory		
Peer-To-Peer Traffic	2	X	Testcard's memory or I/O		
Testcard to System Memory	1	X	System main memory	Locked memory	
CPU to Testcard	1		Testcard's memory or I/O		
CPU and Testcard to System Memory	1				
Busload Generator	1	X	Self		
Master-To-Target Traffic	2	X	Testcard's memory or I/O		
PCI Configuration Scan	1	(X)	All devices on the same bus or on subsequent busses Read only		
Protocol Checker	1 max				
Testcard to System Memory – User Address	1	X	System main memory	Locked memory	
SIG Post Test	1		Testcard's base address registers and the command register.		
SIG Interrupt routing test	1	X	Self		
CPU to Testcard address and Testcard to system address	1	X	Testcard's memory or I/O System main memory	Locked memory	
SIG Cardtest	1	(X)	Complete configuration space of the add-in card, as specified by its device number		
MPTEST– Power Management Test					Part of the SIG Cardtest.
TYPE 1 – Type 1 Test					Part of the PCI Configuration Scan Test.
DISCARD – Discard Test					Part of the Protocol Checker Test.
MCT Test – Maximum Completion Time Test	1		Transfer completion of the add-in card		

NOTE Short descriptions of the tests are also found in the Test Setup window in the GUI where you select your test functions.

Standard Tests

The Agilent System Validation Package includes a series of ready-to-use tests to force the most critical conditions for devices and the system.

Busload Generator

With this test, the PCI or PCI-X testcard simply generates traffic from its master to its own target via the PCI or PCI-X bus. This self-traffic is used to put the bus under stress with additional bus load.

Tested Data Path The tested data path is the PCI or PCI-X bus into which the testcard is plugged.

Tested Devices The tested devices are the arbitration unit and other devices on the same bus.

Recommendations for PCI Testcard Settings The accuracy of the bandwidth setting depends on the use of the PPR feature. To make best use of the busload generator test, there are some recommendations for setting the testcard properties used for this test:

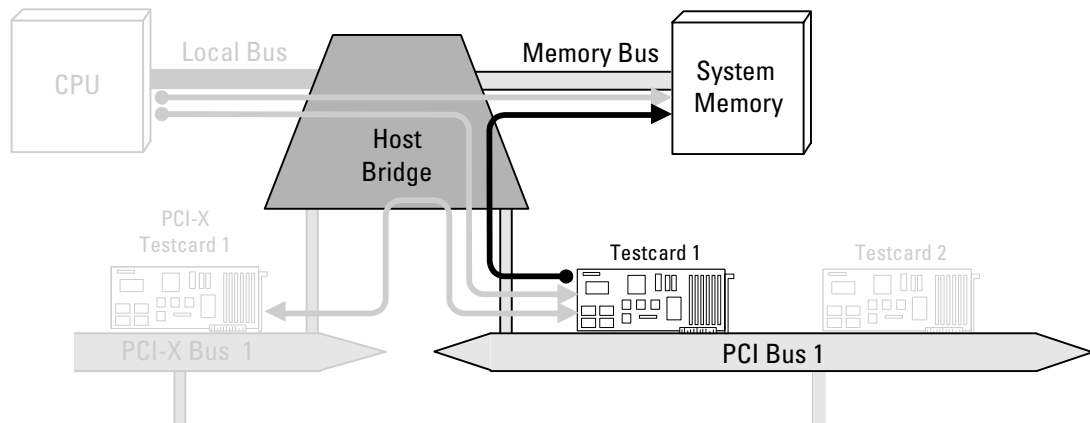
- If you do not need the PPR feature, disable the *Use PPR* check box in the Testcard Setup window.
- If you want to use the PPR feature for the master, select the *Use PPR* check box and set the following target properties:

Property	Value	Description
Termination List (Target PPR Attribute)	0 (noterm)	No termination
Waits List (Target PPR Attribute)	0: for all testcards except E2928/28_Deep 1: for testcard E2928/28_Deep	List of number of waits

For further information on setting testcard properties, refer to *Testcard Setup Window* in the *Agilent E2976A System Validation Package GUI Reference* (pdf-file).

Testcard to System Memory

This test accesses the system memory from the PCI or PCI-X bus. To do this, the testcard is defined as a master and sends different write and read commands.



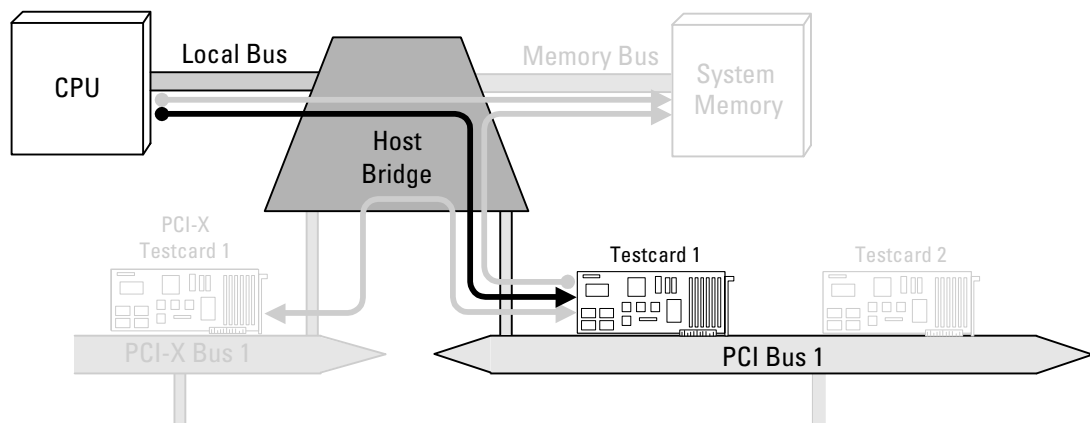
Tested Data Path The tested data path is as follows:

- the PCI/PCI-X bus from the testcard to the host bridge
- the system memory bus from the host bridge to the system memory

Tested Devices The tested devices are the host bridge, the host bridge configuration, the host memory controller and the arbitration unit.

CPU to Testcard

This test accesses either the memory space or the I/O space of the testcard from the CPU. To do this, the test card is defined as a target.



CPU to Testcard Memory Space

Tested Data Path The tested data path is as follows:

- the CPU local bus and
- the PCI/PCI-X bus from the host bridge to the testcard

Tested Devices The tested devices are the host bridge, the host bridge configuration and the host memory controller.

CPU to Testcard I/O Space

The access to the I/O space takes place via a virtual memory buffer and uses the I/O read and I/O write commands only.

Tested Data Path The tested data path is the CPU local bus (I/O access) and the bus from the host bridge to the testcard I/O port.

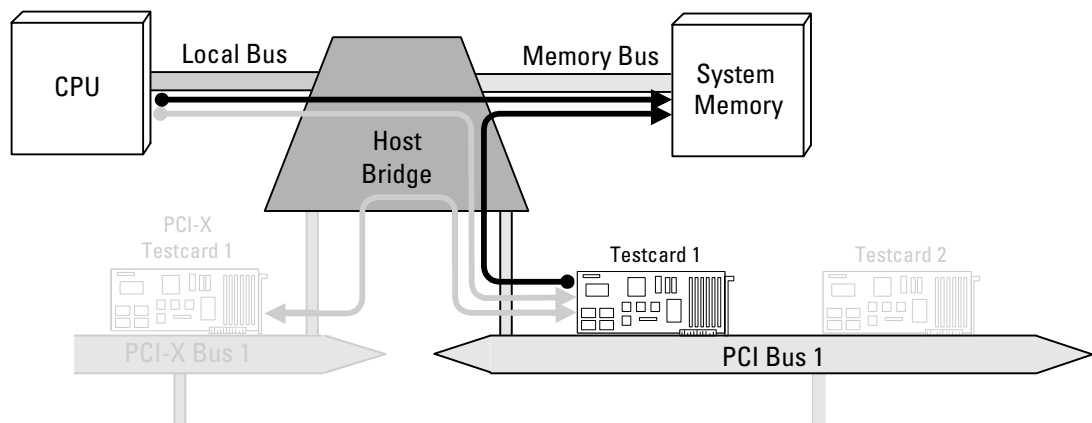
Tested Devices The tested devices are the host bridge, host bridge configuration and the host memory controller.

CPU and Testcard to System Memory

This test accesses the system memory space on two data paths at the same time:

- The CPU accesses system memory space via a virtual memory.
- The master of the testcard accesses system memory through the host bridge.

CPU and testcard perform different read and write commands to system memory. They access the same 4-KB memory page with each device allocated half the page in order to stress the cache controller.



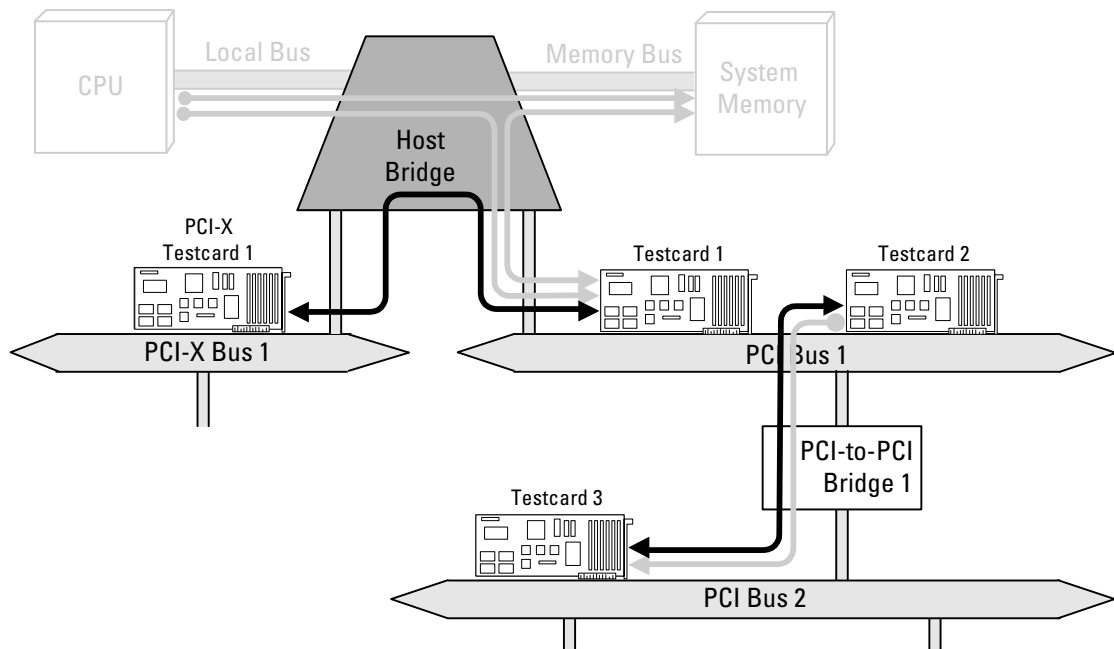
Tested Data Path The tested data path is as follows:

- the CPU local bus
- the PCI/PCI-X bus from the testcard to the host bridge
- the system memory bus from the host bridge to the system memory

Tested Devices The tested devices are the host bridge, the host bridge configuration, the host memory controller, and the arbitration unit.

Peer-To-Peer Traffic

The peer-to-peer test requires two PCI/PCI-X testcards that are set up to access each other's memory space. This is implemented with master to target traffic in both directions. The testcards on different busses are used to test the bridge(s) between them.



Tested Data Path The tested data path is, for example:

- the PCI/PCI-X bus from PCI-X testcard #1 to PCI testcard #1 through the host bridge
- the PCI bus(es) from testcard #2 through the bridge to testcard #3

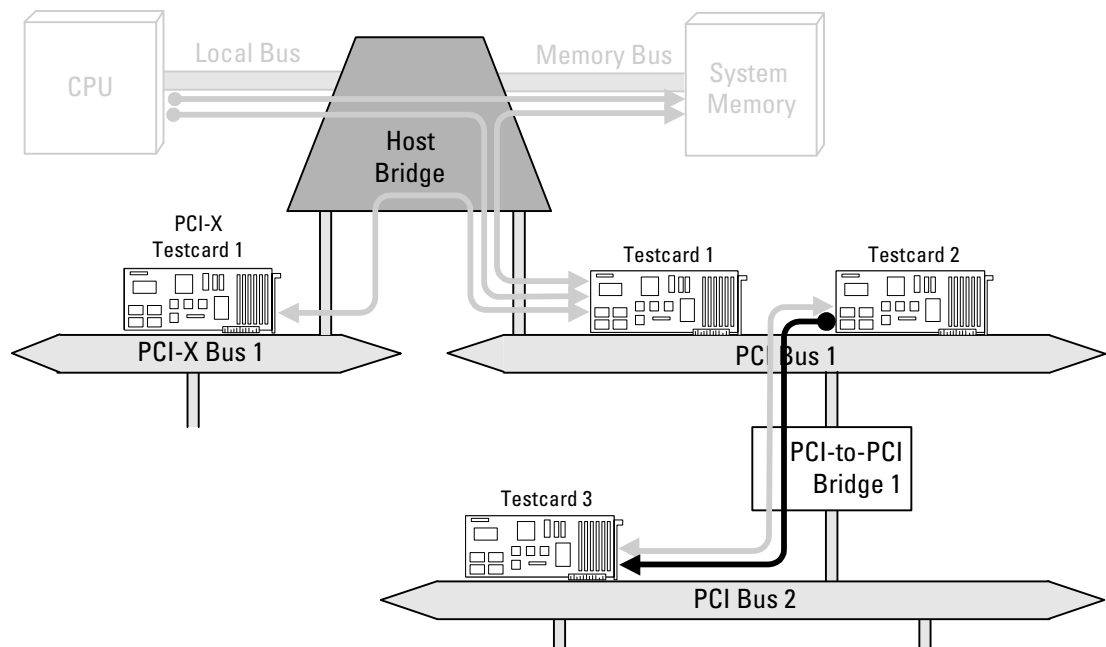
Tested Devices The tested devices are the bridge(s), the bridge configuration(s), and the arbitration unit(s).

NOTE If the selected address space is *MEM* and if PPR is activated, different memory commands (mem_read, mem_readline, mem_readmultiple, mem_writeinvalidate, and mem_write) are permuted.

Master-To-Target Traffic

This test requires two PCI/PCI-X testcards. One testcard accesses the other testcard's memory space. This is implemented with master-to-target traffic in one direction only (in contrast to the Peer-to-Peer test). The testcards on different buses are used to test the bridges in between.

This test can be very helpful, for example, if you have problems with a PCI-to-PCI bridge, and the peer-to-peer test did not pass. Then you can use this test to check both directions separately.



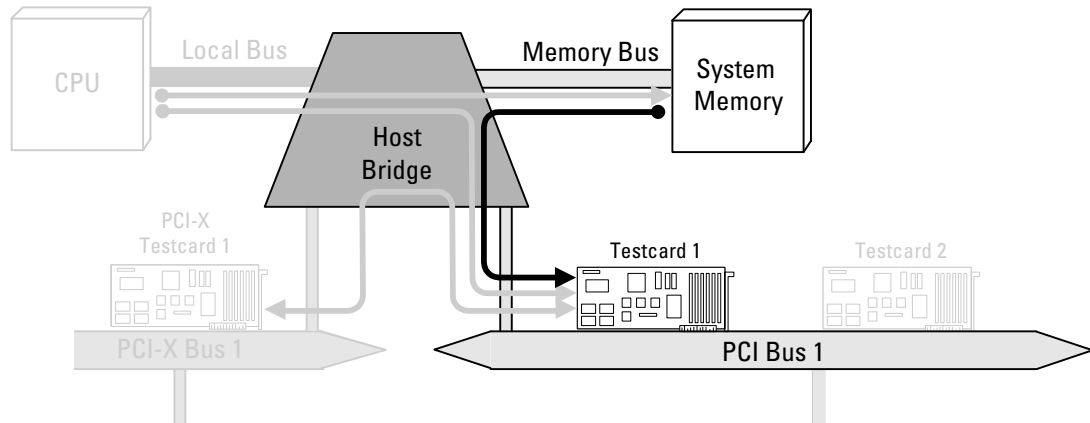
Tested Data Path The tested data path is, for example, the PCI bus(es) from PCI testcard #2 (master) through the bridge(s) to the testcard #3 (target).

Tested Devices The tested devices are the bridge(s), bridge configuration(s), and the arbitration unit(s).

NOTE If the selected address space is *MEM* and if PPR is activated, different memory commands (mem_read, mem_readline, mem_readmultiple, mem_writeinvalidate, and mem_write) are permuted.

Testcard Read from System Memory

The testcard read test is used to check availability/readability of certain memory areas (system memory, device-mapped memory space and I/O space).



Tested Data Path The tested data path is, for example:

- the PCI bus from the host bridge to the PCI testcard #1
- the system memory bus from the system memory to the host bridge

Tested Devices The tested devices are the host bridge, the host bridge configuration, the host memory controller, and the arbitration unit.

Protocol Checker

This test does not drive any transactions on the PCI or PCI-X bus. The testcard only observes the device(s) on the PCI or PCI-X bus by checking PCI or PCI-X protocol violations. The detected problems are logged in the test report.

PCI Configuration Scan

In this test, the testcard actively scans the whole configuration space of the bus. The configuration space report, which is stored in the test report, documents the test conditions during the test run.

Because the configuration space may change with each system reboot, this can be a big help when trying to identify errors that only occur sporadically.

Testcard to System Memory - User Address

Test Description This test is similar to the test “*Testcard to System Memory*” on page 46, but allows you to define the address space memory or I/O and the offset in the system memory. This can be specified in the Test Setup window.

CAUTION

If the operating system is present, execution of this test may cause the system to hang.

Tested Data Path Testcard --> Host/PCI-Bridge --> Host Memory

Tested Devices Host Bridge, Host memory controller, Arbitration Unit

PCISIG Compliance Tests

The Agilent System Validation Package includes a series of tests defined by the PCI Special Interest Group (PCISIG). These tests are used to verify that devices and systems are compliant to the PCI and PCI-X specifications. The tests are set up and run via the System Validation Package combined with either the PCI or PCI-X exerciser/analyzer testcards.

MLT - Master Latency Test

This test is not implemented as a special test within SVP but can be carried out manually. To do this, carry out the PCI configuration scan test (see “*PCI Configuration Scan*” on page 50) and examine the latency settings to determine the result of this test.

SIG Post Test

NOTE This test refers to the PCISIG PCI Post test.

Test Description This test is utilized to initialize the Base Address registers and to verify the address assignments. To do this, the testcard is defined as target.

Test Options Several different sets of test values can be added to a scenario in order to cover different options in one test. Each of the options is shown below. These can be selected after clicking the *Extended Options* button in the Test Setup window for the SIG Post test.

Option	Description
BAR0 Data ... BAR5 Data	Determines the location and type of decoder 0 ... 5, for example, memory and IO.
BAR0 Mask ... BAR5 Mask	Determines the size of the decoder 0 ... 5.
Command Register Data	Determines which bits in the command register are looked at. (Expected data in Command register).
Command Register Mask	Values of the command register.

BAR0 and BAR1, BAR2 and BAR3, and BAR4 and BAR5 can also be used as 64-bit pairs instead of the 32-bit decoders.

The values shown above are used to define the BARs and Command Register. After they have been changed, the system is rebooted to check the configuration.

NOTE It is possible here to enter invalid values. This could be done to test the behavior of the host system's BIOS.

Test Procedure The test procedure is as follows:

1. This test checks to see if there are any overlaps in the address spaces for each of the decoders and tests to see if the decoders are disabled in the BIOS if an overlap error occurs.
2. After the system reboots, the Front Side Interface executable (see *"The Front Side Interface Executable" on page 39*) reports address map errors.
3. The FSI executable also checks to see if the command register is set to the expected values.

SIG Interrupt Routing Test

Test Description The exerciser asserts an interrupt on request from the analyzer mailbox. To do this, the testcard is defined as a master.

The software requests an interrupt from the analyzer and verifies that the interrupt was received and processed correctly.

This test needs the FSI executable and is therefore operating system dependent.

Test Procedure The test procedure is as follows:

1. The test checks that no interrupts are asserted..
2. The SVP tells the FSI executable (see “*The Front Side Interface Executable*” on page 39) to install the interrupt handler for a particular interrupt line.
The interrupt line can be selected by clicking the *Extended Options* button in the Test Setup window.
3. The interrupt is asserted.
4. The Front Side Interface reports if the handler has been successfully called. If any errors occur, these are reported in the test report in the SVP GUI.

The test also checks to see if the interrupt is edge or level sensitive.

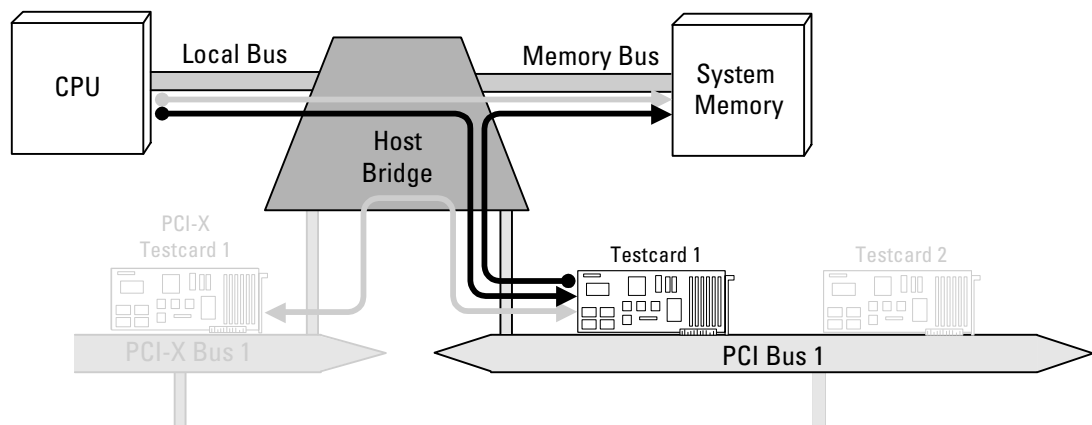
Example Scenario An example of a scenario where the test may fail is if the interrupt handler is not called.

CPU to Testcard Address and Testcard to System Memory Address

Test Description This test accesses either the memory space or the I/O space of the testcard from the CPU. To do this, the testcard is defined as a target.

This test also accesses the system memory from the PCI or PCI-X bus. To do this, the testcard is defined as a master and sends different write and read commands from/to the analyzer.

This test executes the Testcard to System memory and CPU to testcard address space tests at the same time. See *“Testcard to System Memory” on page 46* and *“CPU to Testcard” on page 46*.



This test needs the FSI executable and is therefore operating system dependent.

Tested Data Path The test checks that the system does not hang when traffic is going in different directions between the system and the testcard (PCI bus). The data paths are:

- CPU --> Host/PCI-Bridge --> Testcard memory
- Testcard --> Host/PCI-Bridge --> Host Memory

Tested Devices The test stresses the host bridge.

SIG Card Test

NOTE This test refers to the PCISIG Card Test.

NOTE To carry out the card test for a specific add-in card, you need the device number of this card. This device number must be entered in the respective Card Settings dialog box. The Card Settings dialog box opens when you click the *Extended Options* button in the Test Setup window.

To get the device number of a card on the PCI bus, you can perform a configuration scan test. This can be done by using the TYPE1 - Type 1 Test (Configuration Scan) test. See “*TYPE1 - Type 1 Test*” on page 56 for more information.

Test Description The SIG Card test performs a number of tests. This includes testing for:

- Correct values and operation for the Command Register.
- The Status register.
- Appropriate values for other configuration registers.

The configuration register contents are displayed during the SIG Card test in the SVP Reporting window that opens when you run the test.

Test Procedure The test procedure is as follows:

1. The test carries out a configuration scan of the add-in card and displays all register values.
2. The test checks that the address range of the add-in card is valid.
3. The test then carries out further tests on the command, status and BAR registers—the test checks the complete configuration space of the add-in card.

The Card test also detects if the card is capable of additional power management capabilities and test the current settings. To view and modify the current setting for the power management state delay, click the *Extended Options* button in the Test Setup window.

PMTEST - Power Management Test

NOTE This test refers to the PCISIG power management test.

The PMTEST is covered by the “*SIG Card Test*” on page 55.

TYPE1 - Type 1 Test

This test is covered by the PCI Configuration Scan test. The configuration scan test checks to ensure that the device only shows up once in the system.

Test Description The Type 1 test verifies correct configuration transaction decoding by the device.

Test Procedure In this test, the testcard actively scans the whole configuration space of the bus. The configuration space report, which is stored in the test report, documents the test conditions during the test run.

Because the configuration space may change with each system reboot, this test can provide help when you are trying to identify errors that only occur sporadically.

DISCARD - Discard Test

NOTE This test refers to the PCISIG Discard test.

This test is covered by the protocol checker within the Agilent testcard. Any protocol violations are reported in the report file from the GUI.

Test Description This test verifies that the card correctly repeats retried PCI transactions.

MCT Test - Maximum Completion Time Test

Test Description The Maximum Completion Time test verifies that the system retries transactions within 10 ms.

Test Procedure The test performs the following:

- Sets up the trigger sequencer in the testcard.
- Checks the bus speed.
- Tests to see if the transfer is completed within the number of clock cycles in 10 ms.
- Triggers the analyzer with an error if the transfer does not complete.

Recommendations on Test Duration

NOTE The SIG Post test, the SIG Interrupt Routing test, and the SIG Card test have a test duration of approximately two minutes per test. For the other tests, the test duration can be estimated as described in this section.

The recommended duration of a system stress test strongly depends on the type of the test and even more on the other devices that communicate simultaneously on the system. It is therefore very difficult to estimate test durations.

Estimating Test Durations To estimate test durations, you can check the PPR reports after setting the testcard properties. You can view the PPR reports when you check the syntax of the PPR reports attributes. For further details, refer to *“Check Testcard Settings” on page 66*.

Only System Validation Package Traffic If you are running a single test with the System Validation Package without any other traffic being on the PCI bus, the PPR permutes through all possible combinations within about one minute on 33 MHz busses and about 30 seconds on 66 MHz systems.

If you are running two or more tests of this software on the same bus, the completion of the tests is delayed by the respective factor.

Traffic Caused by Multiple Devices In contrast, if you are testing a system that has other traffic on the bus at the same time, you cannot predict when all possible test conditions will have occurred. The behavior of the System Validation Package is predictable, but the behavior of the other devices is not. These devices might behave “friendly” most of the time. But in many cases you cannot make these devices behave most critically for testing purposes.

If you want to find out whether the system under test can stand these worst-case conditions, or if you want to measure the performance for this case, you have to run much longer tests to reach a high probability that all cases occurred.



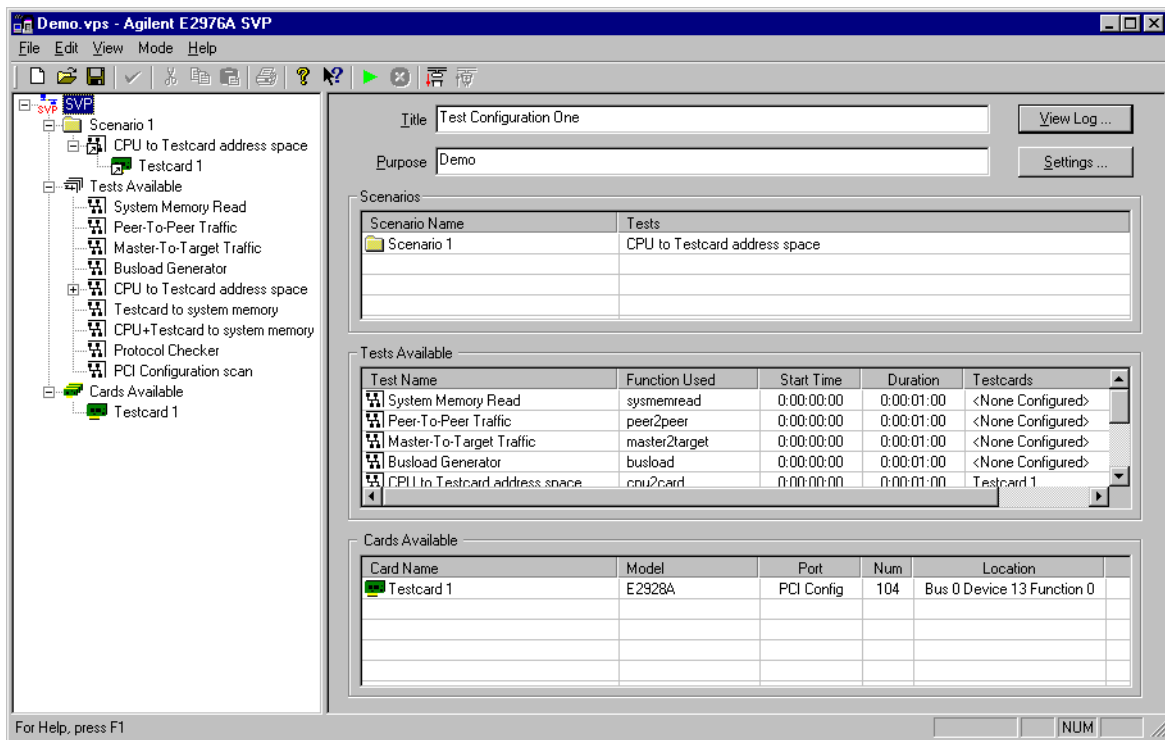
Testing with the User Interface

This section gives information about the test architecture and shows how to set up and define the desired test configuration.

- **Testing Principles**
Overview of the process used to perform a system test.
- **Setting Up the Test Configuration**
Defining scenarios.
- **Defining Test Functions**
Setting test parameters and selecting testcards for each test.
- **Check Testcard Settings**
Opening the Testcard Setup window and checking testcard properties.
- **Running the Test**
Information on the test execution and the test report.

Testing Principles

This section shows the major steps necessary for setting up PCI or PCI-X system tests with the Agilent E2976A System Validation Package. Additionally, you will find information on the different components of the Graphical User Interface (GUI).



Testing with the Graphical User Interface means:

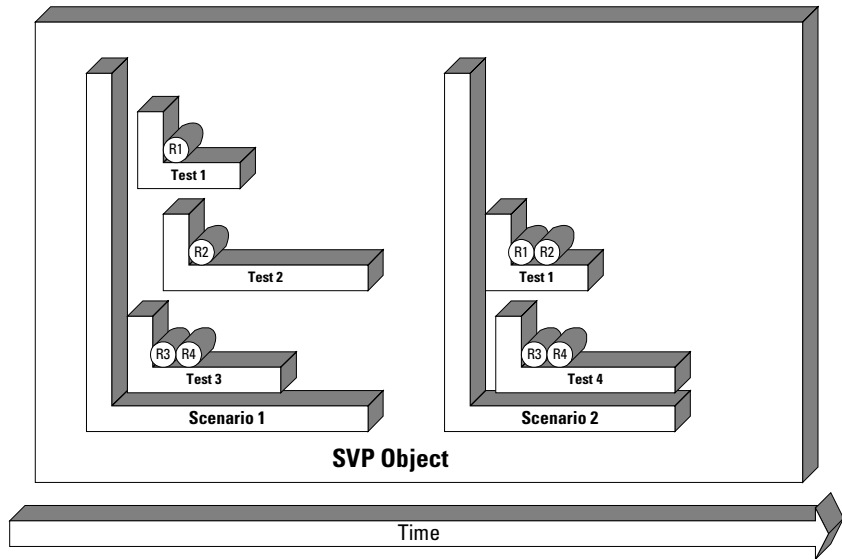
1. Running the System Validation Package

The software automatically scans all connected PCI and PCI-X busses and other control interfaces (RS-232, USB, Fast Host Interface) for Agilent testcards, and tries to initialize the detected testcards. Testcards that could not be initialized are not available for tests. This applies, for example, for testcards that are currently connected to the Agilent E2920 GUI.

If you want to set up a test without any available testcards, you can switch the software into offline mode.

2. Setting up the test configuration

The following figure shows an overview of the test architecture.



The System Validation Package uses a top-down approach to assure testing flexibility. The smallest unit is called a test. It performs one single task, for example, a memory read. The test can use resources such as testcards or processor units (R1, R2, ...).

One step up in the hierarchy is the scenario, which combines several tests for parallel running. Each test and each resource can only be used once per scenario. The scenarios are surrounded by the SVP object, which provides control interfaces for all sub-levels.

There are certain settings at each level of the hierarchy that are also valid for all sub-levels.

See *“Setting Up the Test Configuration”* on page 62 for details.

3. Checking or modifying the properties of the available tests

This step is more or less optional. Basically you can run any test with the default settings. In the case of defining the delay and test duration it is needed to adapt the values. See *“Defining Test Functions”* on page 63 for details.

4. Checking or modifying the properties of the available cards

See *“Check Testcard Settings”* on page 66 for details.

5. Running the test

Click the Run button to start the test. See *“Running the Test”* on page 69 for details.

Setting Up the Test Configuration

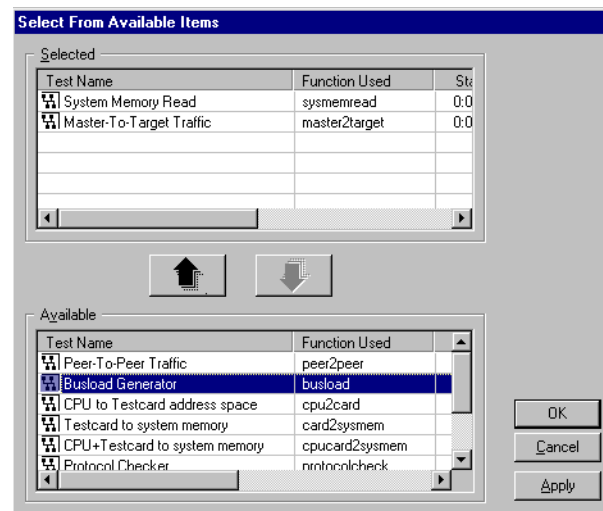
When starting the SVP software, you can find one scenario (Scenario 1) in the SVP object in the navigator (on the left side of the screen).

Add Scenarios to the SVP Object To include further scenarios in the navigator, select the SVP item and click either

- *Insert Scenario* in the shortcut menu, or
- *Insert New Scenario* in the *Edit* menu.

Select Tests in Scenarios To select tests in a Scenario, select the scenario in the navigator and click *Select Test(s)* either from the shortcut menu or from the *Edit* menu.

In both cases, the *Select From Available Items* dialog box is opened. You can now move *Available* tests to the *Selected* tests container and vice versa.



View Scenario Settings You can view settings of one scenario by clicking on the respective scenario in the navigator. This opens the Scenario Details window. This window gives information about the total duration of the current scenario and shows all selected tests.

View the Entire SVP Object You can get an overview of the entire configuration by clicking on the SVP item in the navigator. This opens the SVP Object window.

Defining Test Functions

When starting the SVP software, you will find predefined tests in the *Tests Available* item of the navigator. You can either use these tests for your test configuration or you can create new tests. The new tests can use the same functions as the predefined tests.

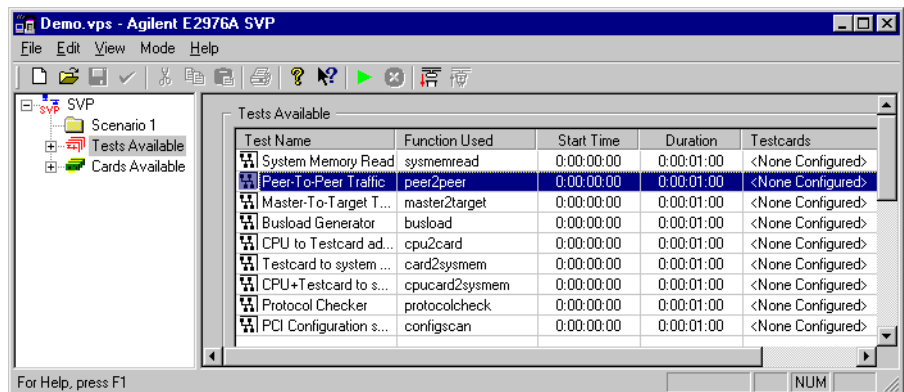
To insert new tests:

- 1 Click the Tests Available item in the navigator.
- 2 Select *Insert Test* in the shortcut menu, or select *Insert New Test* in the Edit menu.

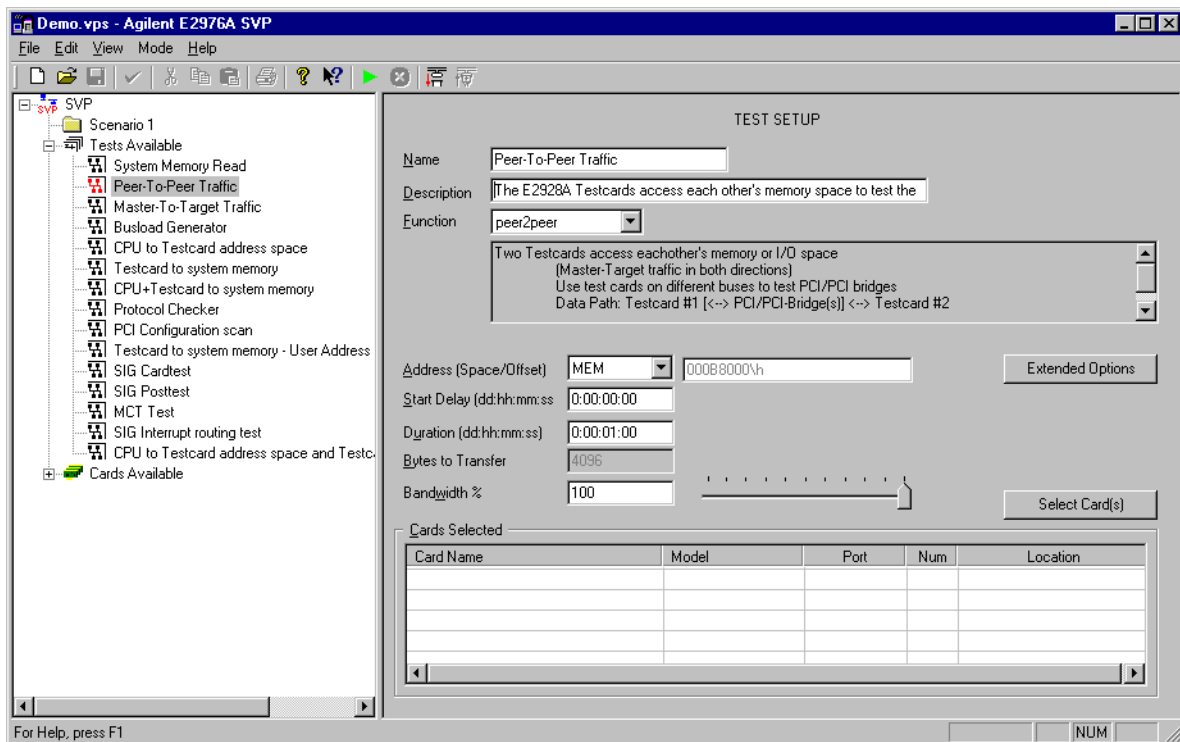
A new test item (for example, Test 1) with predefined settings appears in the navigator and the Tests Available window. The settings can be modified.

View Test Settings To view the settings of one test, you can either

- open *Tests Available* in the navigator and click the respective test item, or
- click *Tests Available* in the navigator. This opens the Tests Available window where you can double-click the test you want to define.

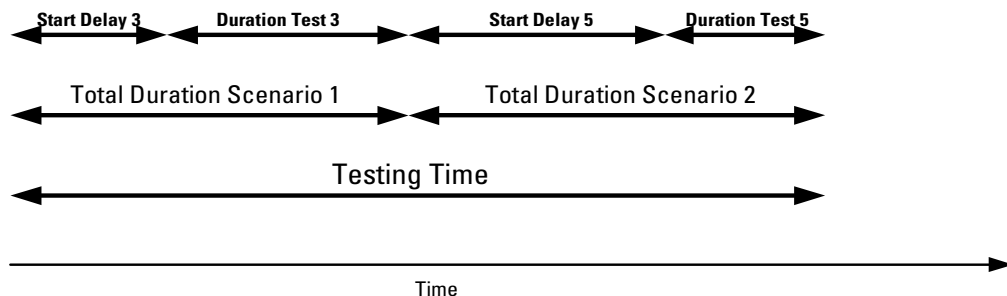


In both cases, the Test Setup window of the respective test is opened.



Here you can modify the current test settings (you can select another test function, for example) and specify the testing time.

The testing time is the sum of the total durations of all scenarios. The total duration is the maximum period of time of the start delay and duration defined for each test in this scenario. These values can be defined in the Test Setup window.



For detailed explanations of all test settings, refer to the *Agilent E2976A System Validation Package GUI Reference* (pdf-file).

Remove Available Tests If there are tests in the Available Tests window that are not needed for the test configuration setup, you can remove them.

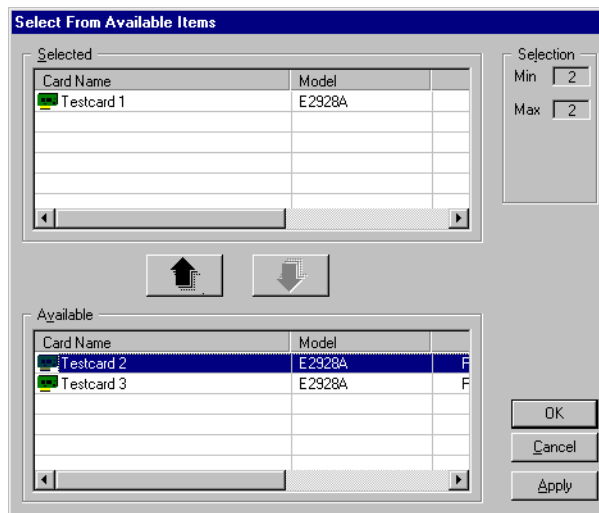
To remove tests from the Available Tests window:

- 1 Select the respective test in the *Tests Available* item in the navigator.
- 2 Select *Remove Test* in the shortcut menu or in the Edit menu.

Select Testcards Each test needs a minimum number of testcards. To assign testcards to the currently selected test, you can either

- click *Select Card(s)* button in the current Test Setup window, or
- use the shortcut menu of the selected test and click *Select Card(s)*, or
- click *Select Card(s)* in the Edit menu.

In all cases, the *Select From Available Items* dialog box is opened. You can now move *Available* testcards to the *Selected* testcards container and vice versa.



For further information, refer to the *Agilent E2976A System Validation Package GUI Reference* (pdf-file).

For checking the testcard settings of all available testcards, refer to “*Check Testcard Settings*” on page 66.

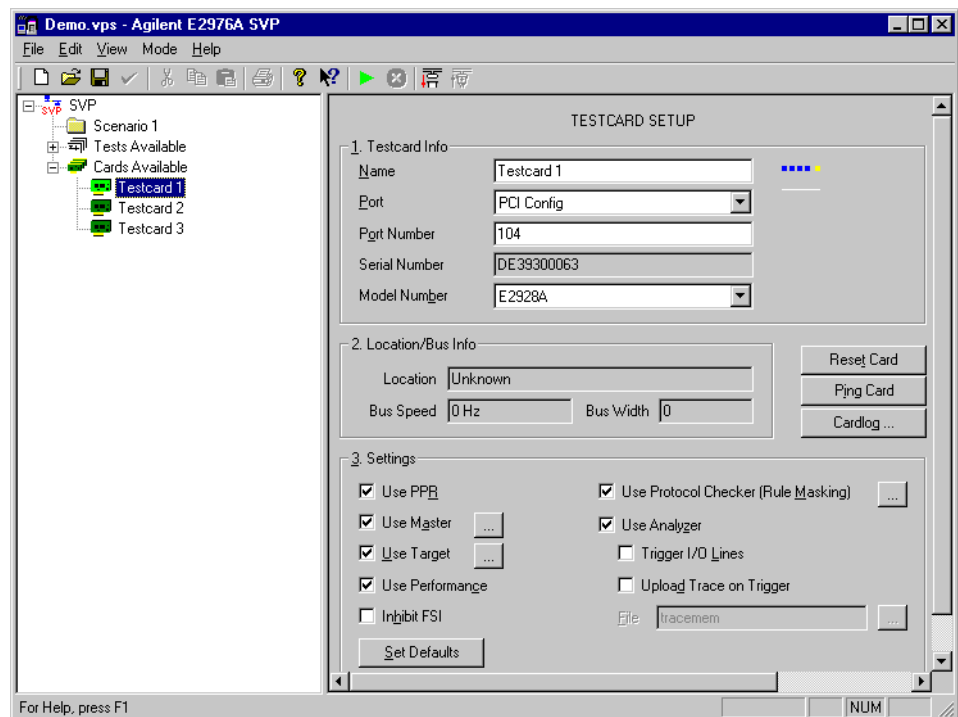
Check Testcard Settings

To view the settings of the available cards, you can either

- open *Cards Available* in the navigator and click the respective testcard, or
- click *Cards Available* in the navigator.

This opens the Testcards Available window where you can double-click the testcard you want to check.

In both cases, the Testcard Setup window of the respective testcard is opened.



The parameters in the *Testcard Info* group and the *Location/Bus Info* group can only be modified in offline mode.

You can modify all current testcard settings under *Settings*. Here you can enable and disable card features (PPR, master, target, performance, FSI, protocol checking and analyzer features). Clicking the details buttons next to the *Use Master* and *Use Target* check boxes shows the available testcard properties that can be modified.

Testcard Features

Master and Target The testcard's exerciser consists of the master and target, and the data memory and data compare unit. Both master and target are programmed and set up automatically for the various tests (except protocol checker) and are not directly accessible as in the E2920 software. Behavior of the two parts can be specified by various property settings.

Analyzer The testcard's analyzer part includes the protocol observer, trace memory, performance counters and trigger in/out capabilities.

- **Protocol Checker**

The testcard's protocol checker continuously monitors the bus and checks for violations of predefined protocol rules, which are partly defined by the PCI and the PCI-X specification and partly by Agilent. Each individual rule can be masked out and will then neither trigger the trace memory nor appear in any report. To mask rules, click the details button next to the *Use Protocol Checker (Rule Masking)* check box.

NOTE Because a testcard can be used in several scenarios, an automatic rule masking is performed on a per-test basis. That means that the user setting of the mask is restored prior to each test.

- **Trace Memory**

Testcard's trace memory is set up to trigger on:

- protocol violations

Masked rules will not trigger the trace memory, and disabling of the observer disables triggering on any protocol rule.

- data compare errors

- bus hang

Too many retries without transfers.

- trigger-in event

See external triggering, below.

- **Performance Measurement**

To monitor system performance, each testcard measures two sets of performance metrics: one for the whole bus, and one for the performance of testcard transactions.

- External/Cross Triggering

To facilitate triggering of external measurement devices, and to enable you to trigger other testcards in the system for a *snapshot* whenever an error occurs, the testcards are set up to use the external trigger lines that must be connected to reflect their internal triggering state. That is, whenever the testcard's trace memory triggers, a trigger-out signal is generated. All trigger-in lines are monitored and used to trigger the card's trace memory.

Which trigger-out line is used for triggering is determined by the testcard's bus number. Therefore, only one testcard per bus needs to be used for cross-triggering.

To find out which trigger-out line is used, use the following formula:

```
triggerline := bus number MOD 12
```

Example:

```
bus number is 16 -> trigger line is 4;
```

```
bus number is 5 -> trigger line is 5; ...
```

Estimating Test Durations

When the PPR feature is active (the *Use PPR* check box is selected), you can estimate test durations by using PPR reports for master and target testcard settings.

For that purpose, view the respective reports by opening the *Card Settings* dialog boxes and clicking the *Check Syntax* button. If the syntax is ok, the PPR report is displayed. Here you can find the parameters (for example, the estimated testing time for one attribute page) needed to estimate the duration of one test function. (Test durations are set in the Test Setup window.)


For further information on testcard settings, refer to the *Agilent E2976A System Validation Package GUI Reference* (pdf-file).

Running the Test

After you have successfully set up your test configuration, all information that is known about the software, the system, the test setup and the type of test hardware is listed in the static report. You can view this report by clicking *Static Report ...* in the View menu.

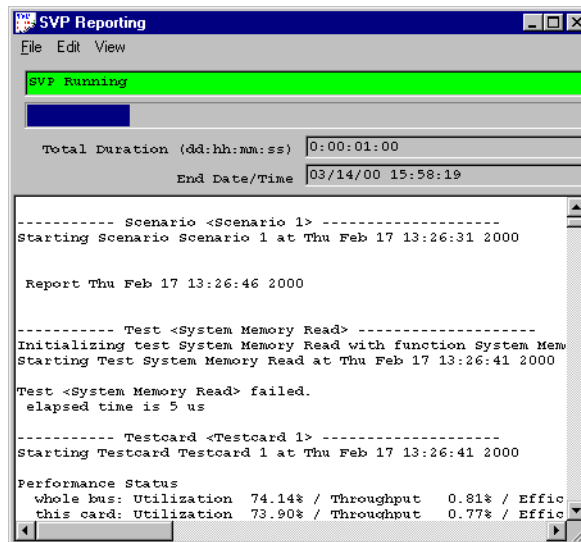
Before you run a test ensure that you are in online mode. If not, click *Go Online* in the *Mode* menu.

To run the test configuration, click either

- the *Run* icon  in the toolbar, or
- *Run* in the shortcut menu, or
- *Run* in the File menu.

When the test is started, the SVP software automatically selects the SVP object in the navigator and opens the SVP Reporting dialog box. You can now view the status of the current test and the test report.

For details on the test report, refer to the *Agilent E2976A System Validation Package GUI Reference* (pdf-file).



Status of the Testing	<p>The following messages can appear in the status line of the SVP Reporting dialog box:</p> <p>SVP Initializing Test The specified test is currently being initialized.</p> <p>SVP Running The test is running.</p> <p>SVP Stopped The test has finished. If errors occurred, they are listed in the test report.</p> <p>SVP Error! The test has stopped due to a detected error. The error is listed in the test report.</p>
Error Types	<p>The <i>CardLog</i> report provides additional information on the type of errors that have been detected. Possible errors are protocol violations, errors in data comparison or master abort conditions. These errors will also be reported in the test report.</p>
Performance	<p>You can also view the performance of the system under test during the test run. The performance is displayed in terms of utilization, data throughput and efficiency for the whole bus and for the current card. These values are displayed during run time, but are not stored in any report file. For detailed explanations of these measures, refer to <i>Predefined Performance Measures</i> in the <i>Analyzer User's Guide</i> (pdf-file), which is delivered with the testcard.</p>



Test Results

This section briefly explains the results of the system tests provided with the Agilent E2976A System Validation Package. It covers the contents of the different output files as well as some error handling instructions.

For information on:

- the log file, refer to the “*Log File Description*” on page 72.
- the PPR report files, refer to the “*Report File Description*” on page 73.
- the error handling, refer to “*Error Handling*” on page 74.

Log File Description

The log file is opened when the System Validation Package is started. The default name is `svp.log` and the default location is the reports subdirectory in the SVP directory.

View the Log File To view the log file, click the *View Log ...* button in the SVP Object window.

Log File Contents The log file includes:

- The start date and time of the test session.
- All tests that were run during the session including their
 - test start date and time,
 - type of test,
 - test termination with the results, either *passed* or *failed*,
 - the elapsed time of the test.
- All testcards that are used during the session including their
 - start date and time,
 - testcard status (performance, observer, trace memory trigger),
 - testcard configuration.
- Test results for each testcard after a scenario has been finished including
 - maximum performance,
 - protocol checker results.
- Total elapsed time for each scenario.

Report File Description

The output functions of the PCI and PCI-X Protocol Permutator & Randomizer create several report files for each test action in your test scenario. They contain detailed information about all the PPR functions that were called during the tests.

Report Files

The PPR report files are:

- Master Block file
This file contains the settings of all generic PPR properties and master block permutation properties.
- Master Attribute file
This file contains the settings of all generic PPR properties and master attribute permutation properties.
- Target Attribute file
This file contains the attribute settings for the target.

The PPR report file names can be defined in the testcard settings (see *Testcard Setup Window* in the *Agilent E2976A System Validation Package GUI Reference* (pdf-file)).

Report File Contents

The contents of the PPR report files are fairly complex and you should not need to open them to interpret your test results. However, for a detailed analysis of your test specification and the results, they are provided with the System Validation Package.

For a complete explanation of the report file contents, please refer to the *Agilent C-API/PPR Programmer's Guide*, which is delivered with the testcard.

Error Handling

This section is not meant to be a complete troubleshooting guide. It lists some of the errors that might occur on some systems and that are relatively easy to handle.

Test Function Errors Every test function within the test scenarios uses the PCI or PCI-X Analyzer to trigger at certain error events. The different types of errors that may occur with this tool are:

- PCI or PCI-X protocol errors
One of the PCI or PCI-X protocol rules has been violated.
- Data compare errors
An error has occurred in the transferred data.
- Master abort condition

The GUI allows you to define whether the tests continue after an error. This can be done in the SVP Test Settings dialog box, which can be accessed via the SVP Object window.

To narrow down the problem with the tested devices, it may help to test the same data path with another test action.

For example, if you have problems with the communication over a PCI/PCI bridge using the “Peer-to-Peer Traffic” test, you could examine both directions separately with two “Master-to-Target Traffic” tests to find out if the errors occur in one direction only.

Testcard Errors One of the following testcard errors may occur:

- Testcards detection errors
When the program is started, it scans the system under test for Agilent testcards.
However, you can reset these testcards to factory defaults—including both memory and I/O space—in the Testcard Setup window. In both cases these testcards are excluded from tests until the system is rebooted.
For more information on the handling of testcard detection errors, please refer to the C-API description in the user’s guide (pdf-file), which is delivered with the respective testcard.

- Errors during test run

If the error occurred during test run, the *Cardlog* in the program window displays the status *Error*. The function that caused the error is logged in the SVP Reporting dialog box where the Cardlog is displayed. In this case, too, a card reset and reboot may help.

For more information on the handling of errors during test run, please refer to the *Agilent C-API/PPR Programming Reference*, which is delivered with the respective testcard.

- PPR errors

If the testcard error was detected by the PPR, its name starts with *B_E_PPR*. Please refer to the *Agilent C-API/PPR Programming Reference*, which is delivered with the respective testcard.

Common Protocol Errors

The Analyzer of the Agilent testcard observes 53 different protocol rules on the PCI bus and 53 protocol rules on the PCI-X bus, and triggers the trace memory if any violation of these rules occurs. A violation of some of these rules, however, does not always cause problems. In fact, on some machines, protocol errors occur regularly. An example is the rule LAT0 (the Target Ready signal is not asserted within 16 clock cycles after Initiator Ready was asserted).

In the system default configuration, these protocol errors will also terminate the test, even if there is no problem on the bus.

To keep these protocol errors from terminating a test for a particular protocol rule:

- 1 Determine the testcard(s) that detected the error and open the respective Testcard Setup window, for example by clicking on this testcard in the navigator.
- 2 Click the details button next to the selected *Use Protocol Checker (Rule Masking)* check box to open the Protocol Rule Masking dialog box.
- 3 Disable the respective rule by toggling its enabled/disabled field.
- 4 Repeat these steps for all testcards that detected this error.

Setup File Reference

All settings of the System Validation Package 2.1 can easily be set or modified by the user via the Graphical User Interface (GUI). The settings have reasonable default values.

The settings file has the following structure:

- Test configuration
Information about the software version, inserted scenarios, operation mode, name of the log file, testcard identifier, title and purpose of the test configuration.
- Test sequence configuration
Information about inserted scenarios and tests.
- Settings of the available tests
Test settings are introduced by the name of the test in brackets (for example, [Test System Memory Read]).
- Settings of the available testcards
Testcard settings are introduced by the testcard name in brackets (for example, [Testcard Testcard 1]).

You can save your GUI configuration settings to a VPS file. This file can be loaded by using the *Load* feature in the GUI.

The VPS file is in plain ASCII format and can be edited with any standard text editor.

For more information, especially on PPR settings, please refer to the *Agilent C-API/PPR Programming Reference*, which is delivered with the respective testcard.

Settings File Formats

The settings file contains a set of properties, following the syntax below:

```

<settings file>      :   <header> <scenario info>+ <test info>+ <card info>*
<header>             :   <setting>+
<scenario info>      :   "[scenario" <scenario name> "]" <setting>+
<test info>          :   "[test" <test name> "]" <setting>+
<card info>          :   "[testcard" <card name> "]" <setting>+
<scenario name>      :   unquoted string
<test name>          :   unquoted string
<testcard name>      :   unquoted string
<setting>            :   <property name> "=" <property value>
<property name>      :   see tables below
<property value>     :   <DWORD value> | <string value> | <address value> |
                        <boolean value>
<DWORD value>        :   hex format (0x1234 or 1234\h), decimal format (1234),
                        binary format (011\b)
<string value>       :   quoted string
<address value>      :   "<" ( "MEM" | "IO" | "CONF" ) ":" [<hi-addr>] <hi-addr> ">"

```

Example

```

[Test System Memory Read]
starttimeoffset = 0\h
duration = 3c\h
address.space = mem
function = "systememread"
address = <MEM:000B8000\h>
bandwidth = 64\h
size = 1000\h
description = "This is the text"
items.list = "Testcard 1"

```

Scenario and Test Parameter

Scenario Property Scenarios allow several tests to be run concurrently. Any testcard can only be used once per scenario. Scenarios have no special settings except for the list of tests that are used.

Scenario Property used in the GUI	Scenario Property used in the Settings File	Values	Description
Scenario	items.list	string list	List of tests (by names) that are used in this scenario

Test Properties All tests share some or all of the following properties:

Test Property used in the GUI	Test Property used in the Settings File	Values	Description
Address Offset	address	address value	Physical address of the memory
Address Space	address.space	"mem" or "io"	Memory space or I/O space is used
Bytes to Transfer	size	DWORD	Size of the memory (in bytes) that is use.
n/a	address.prefetch	True or False	The pre-fetchable decoder is used if available
Bandwidth %	bandwidth	0 ... 100	Value of the maximum bandwidth Note: Using a bandwidth < 1.0 will cause that the PPR testcard setting B_M_DELAY is overridden.
Description	description	string	User-defined description
Function	function	string	Short name of test function
Start Delay	starttimeoffset	DWORD	Start Delay in seconds (from start of scenario)
Duration	duration	DWORD	Duration of the test (in seconds)

Testcard Parameters

Testcard parameters can be divided into:

- Testcard and Location Information
- Card Features Settings
- Master Settings (for PCI Testcards)
- Target Settings (for PCI Testcards)
- Requester Settings (for PCI-X Testcards)
- Completer Settings (for PCI-X Testcards)
- Protocol Checker (Rule Masking)

Testcard and Location Information

Card Property used in the GUI	Testcard Property used in the Settings File	Type	Range	Description
Serial Number	card.serialnumber	string	valid serial number	Serial number of the testcard
Port	connection.port	port string	rs232 fhif pci usb (PCI-X only)	Connection port of the testcard
Port Number	connection.portnum	DWORD	depends on port	Connection port number
Model Number	card.model	string	valid models	Model number of the testcard
Location	card.location	string	valid locations	Location of the testcard (for example, Bus 0 Device 13 Function 0)

Card Features Settings

Card Property used in the GUI	Testcard Property used in the Settings File	Type	Range	Description
Use Performance	use.performance	boolean	True or False	Performance counters of the testcard are enabled or disabled
Use Protocol Checker (Rule Masking)	use.observer	boolean	True or False	Protocol Observer of the testcard is enabled or disabled
Use Master	use.master	boolean	True or False	Master of the testcard is enabled or disabled
Use Target	use.target	boolean	True or False	Target of the testcard is enabled or disabled
Use PPR	use.ppr	boolean	True or False	Attribute permutation is enabled or disabled
Use Analyzer	use.tracememory	boolean	True or False	Analyzer of the testcard is enabled or disabled
Use Trigger I/O Lines	use.triggerio	boolean	True or False	Cross-triggering is enabled or disabled
Upload Trace on Trigger	tracememory.upload	boolean	True or False	Trace memory upload is enabled or disabled
n/a	tracememory.trigger.proterr	boolean	True or False	Trace memory trigger on protocol error is enabled or disabled
n/a	tracememory.trigger.datacmp	boolean	True or False	Trace memory trigger on data compare error is enabled or disabled
n/a	tracememory.trigger.bushang	boolean	True or False	Trace memory trigger on bushang is enabled or disabled
n/a	tracememory.trigger.spliterr	boolean	True or False	Trace memory trigger on split error is enabled or disabled
Inhibit FSI	inhibit.fsi	boolean	True or False	Inhibit connection to FSI on host
File	tracememory.upload.file	string		Name of the file to which the card's trace memory is written (without extension)
n/a	performance.measure	DWORD	0 ... 7	Measure used by performance
n/a	performance.cardmeasure	DWORD	0 ... 7	Measure used by card's performance

Master Settings (for PCI Testcards)

Card Property used in the GUI	Testcard Property used in the Settings File	Type	Range	Description
n/a	master.blockpage	DWORD	0 ... 16	Blockpage used by the master
Write Command	master.block.cmd.write	DWORD	mem_write, mem_ writeinvalidate	PCI bus command for the block transfer (mem)
Read Command	master.block.cmd.read	DWORD	mem_read, mem_readline, mem_ readmultiple	PCI bus command for the block transfer during address phase (mem)
Master Internal Address	master.address.internal	DWORD	0 ... size of data memory	Internal address of the testcard's data memory; used by the master
Block Size List (Master PPR)	ppr.master.block.size.list	string	Multiple of 4 in the range of 4 ... 128k	List of numeric values for block sizes, measured in bytes
Block Algorithm (Master PPR)	ppr.master.block.alg	DWORD	0 ... 3	Algorithm used to pick values from the value list of master block properties
Block Byte Enable List (Master PPR)	ppr.master.block.byten.list	string	0 ... 15	List of numeric values for C/BE byte enables
Block Commands List (Master PPR)	ppr.master.block.cmds.list	DWORD	0 ... 15	List of PCI bus commands used for permutations
Block Alignment List (Master PPR)	ppr.master.block.align.list	string	<i>Granularity:</i> Power of 2 between cacheline size and 8192. <i>Offset:</i> Multiple of 4 between 0 and 8188	Granularity and offset within this granularity that restrict the start of a block
PPR Report (Master Block)	ppr.master.block.report	boolean	True or False	Writing of the PPR report is enabled or not
PPR Block Report File (Master Block)	ppr.master.block.report.file	string		Name of the file used for the PPR report or master block permutations
Master Attribute Page (memory)	master.attrpage.memory	DWORD	0 ... 63	Attribute page used for access to the memory space by testcard
Master Attribute Page (i/o)	master.attrpage.io	DWORD	0 ... 63	Attribute page used for access to the I/O space by testcard
Waits List (Master PPR Attribute)	ppr.master.attr.waits.list	string	0 ... 30	List of numbers of waits
Burst Length List (Master PPR Attribute)	ppr.master.attr.last.list	string	0 ... 2 ³²	List of last phases of bursts (this is, burst lengths)
Release Request (Master PPR Attribute)	ppr.master.attr.rreq.list	string	0 ... 15	List of number of cycles after which REQ# is released after assertion of FRAME#

Card Property used in the GUI	Testcard Property used in the Settings File	Type	Range	Description
DPERR List (Master PPR Attribute)	ppr.master.attr.dperr.list	string	0 or 1	List of parity errors, signaled or not signaled
SPERR List (Master PPR Attribute)	ppr.master.attr.dserr.list	string	0 or 1	List of system errors in the data phase, signaled or not signaled
APERR List (Master PPR Attribute)	ppr.master.attr.aperr.list	string	0 or 1	List of system errors in the address phase, signaled or not signaled
DWRPAR List (Master PPR Attribute)	ppr.master.attr.dwp.list	string	0 or 1	List of wrong parities set one clock after a write data transfer, inverted or not inverted
AWRPAR List (Master PPR Attribute)	ppr.master.attr.awp.list	string	0 or 1	List of wrong parities set one clock after the address phase, inverted or not inverted
WAITMODE List (Master PPR Attribute)	ppr.master.attr.waitmode.list	string	0 or 1	List of values to keep the address constant during the WAITS phases or not
STEPMODE List (Master PPR Attribute)	ppr.master.attr.stepmode.list	string	0 or 1	List of values to keep the address constant during the STEPS phases or not
STEPS List (Master PPR Attribute)	ppr.master.attr.steps.list	string	0 or 1	List of numbers of additional clocks during an address phase They are added between assertion of GNT# and assertion of FRAME#.
TRYBACK List (Master PPR Attribute)	ppr.master.attr.tryback.list	string	0 or 1	List of Fast Back-to-Back cycle tries (only available for E2925B, E2926A/B, E2927A and E2940A)
DELAY List (Master PPR Attribute)	ppr.master.attr.delay.list	string	2 ... 2 ²¹	List of numbers of clocks a master transaction is delayed before its start Note: Delay will be modified if bandwidth < 100 % (specified in test).
REQ64 List (Master PPR Attribute)	ppr.master.attr.req64.list	string	0 or 1	List of 64-bit transfer tries
AWRPAR64 List (Master PPR Attribute)	ppr.master.attr.awp64.list	string	0 or 1	List of wrong parities (PAR64) set one clock after the address phase, inverted or not inverted
DACWRPAR (Master PPR Attribute)	ppr.master.attr.dacwp.list	string	0 or 1	List of wrong parities signaled in the second cycle of a dual address cycle, inverted or not inverted
DACWRPAR64 (Master PPR Attribute)	ppr.master.attr.dacwp64.list	string	0 or 1	List of wrong parities (PAR64) signaled in the second cycle of a dual address cycle, inverted or not inverted
DACPERR List (Master PPR Attribute)	ppr.master.attr.dacperr.list	string	0 or 1	List of system errors in the second cycle of a dual address cycle, signaled or not signaled

Card Property used in the GUI	Testcard Property used in the Settings File	Type	Range	Description
DWRPAR64 List (Master PPR Attribute)	ppr.master.attr.dwp64.list	string	0 or 1	List of wrong parities (PAR64) set one clock after a write data transfer, inverted or not inverted
RESUMEDELAY List (Master PPR Attribute)	ppr.master.attr.resumelay.list	string	2 ... 127	List of clock numbers after which the master resumes after a target termination
PPR Report (Master Attribute)	ppr.master.attr.report	boolean	True or False	Writing of the PPR report is enabled or not
PPR Report	ppr.report	boolean	True or False	Writing of the PPR report is enabled or not
PPR Report File	ppr.report.file	boolean	True or False	Name of the file used for the PPR report of completer permutations

Target Settings (for PCI Testcards)

Card Property used in the GUI	Testcard Property used in the Settings File	Type	Range	Description
Target Attribute Page Number	target.attrpage	DWORD	0 ... 63	Attribute page used by the target
Termination List (Target PPR Attribute)	ppr.target.attr.term.list	string	0 ... 3	List of termination modes, for example, "32*noterm, 2*retry, disconnect, abort"
WAITS List (Target PPR Attribute)	ppr.target.attr.waits.list	string	0 ... 30	List of number of waits
DPERR List (Target PPR Attribute)	ppr.target.attr.dperr.list	string	0 or 1	List of parity errors, signaled or not signaled
SPERR List (Target PPR Attribute)	ppr.target.attr.dserr.list	string	0 or 1	List of system errors in the data phase, signaled or not signaled
APERR List (Target PPR Attribute)	ppr.target.attr.aperr.list	string	0 or 1	List of parity errors in the address phase, signaled or not signaled
WRPAR List (Target PPR Attribute)	ppr.target.attr.wp.list	string	0 or 1	List of wrong parities set one clock after a write data transfer, inverted or not inverted
ACK64 List (Target PPR Attribute)	ppr.target.attr.ack64.list	string	0 or 1	List of 64-bit requests, acknowledged or not acknowledged
Target Attribute DACPERR List	ppr.target.attr.dacperr.list	string	0 or 1	List of address parity errors, signaled or not signaled
Target Attribute WRP64 List	ppr.target.attr.wp64.list	string	0 or 1	List of wrong parities set one clock after a write data transfer, inverted or not inverted
Target Attribute Report	ppr.target.attr.report	Boolean	True or False	Writing of the PPR report is enabled or not
Target Attribute Report File	ppr.target.attr.reportfile	string		Name of the file used for the PPR report or target attribute permutations

Requester Settings (for PCI-X Testcards)

Card Property used in the GUI	Card Property used in the Settings File	Type	Range	Description
BUSCMD List (RI PPR Block)	ppr.ri.blk.buscmd.list	DWORD	0 ... 15	List of PCI-X bus commands used for permutations
BYTEN List (RI PPR Block)	ppr.ri.blk.byten.list	string	0 ... 15	List of numeric values for byte enables This parameter is only valid for block transfers with the command <i>memwrite</i> .
ALIGN List (RI PPR Block)	ppr.ri.blk.align.list	string	0 ... 7	List of alignments to QWORD boundary
NUMBYTES List (RI PPR Block)	ppr.ri.blk.numbytes.list	string	0 ... MaxDWord	List of number of bytes in the current block
RELAXORDER List (RI PPR Block)	ppr.ri.blk.relaxorder.list	string	0 or 1	List of relaxed ordering bits (relaxed ordering is done or not done)
NOSNOOP List (RI PPR Block)	ppr.ri.blk.nosnoop.list	string	0 or 1	List of bits that signify whether no snoop will be done
BYTECOUNT List (RI PPR Behavior)	ppr.ri.beh.bytecount.list	string	0 ... 4096	List of numeric values for byte counts. Sequences are generated with these byte counts
DISCONNECT List (RI PPR Behavior)	ppr.ri.beh.disconnect.list	string	0 ... 32	List of values that determine whether and how often a requester-initiator will disconnect its current sequence
DELAY List (RI PPR Behavior)	ppr.ri.beh.delay.list	string	1 ... 65535	List of numbers of clock delays
STEPS List (RI PPR Behavior)	ppr.ri.beh.steps.list	string	0 ... 32	List of address steps numbers
REQ64 List (RI PPR Behavior)	ppr.ri.beh.req64.list	string	0 or 1	List of 64-bit data transfer tries
RELREQ List (RI PPR Behavior)	ppr.ri.beh.relreq.list"	string	1 ... 2047	List of number of cycles after which REQ# is released after assertion of FRAME#
DECSPEED List (RT PPR Behavior)	ppr.rt.beh.decspeed.list"	string	A, B, C	List of decode speeds

Card Property used in the GUI	Card Property used in the Settings File	Type	Range	Description
ACK64 List (RT PPR Behavior)	ppr.rt.beh.ack64.list	string	No, Yes	List that determine s whether a 64-bit data transfer acknowledge will be asserted or will not be asserted
INITIAL List (RT PPR Behavior)	ppr.rt.beh.initial.list	string	Accept Single Retry TAbort	List that determines the initial behavior of the requester-target response
LATENCY List (RT PPR Behavior)	ppr.rt.beh.latency.list	string	3 ... 34	List of numbers of initial latency clocks
SUBSEQ List (RT PPR Behavior)	ppr.rt.beh.subseq.list	string	0 or 1	List that specifies the target response in subsequent data phases 0: accepts all subsequent data phases 1: disconnects in the selected data phase
SUBSEQPHASE List (RT PPR Behavior)	ppr.rt.beh.subseqphase.list	string	0 ... 2047	List of selected subsequent data phases

Completer Settings (for PCI-X Testcards)

Card Property used in the GUI	Card Property used in the Settings File	Type	Range	Description
PPR Report	ppr.report	boolean	True or False	Writing of the PPR report is enabled or not
PPR Report File	ppr.report.file	boolean	True or False	Name of the file used for the PPR report of completer permutations
PARTITION List (CI PPR Behavior)	ppr.ci.beh.partition.list	string	0 ... 63	List that defines the sizes of the (partial) completion transactions.
ERRMESSAGE List (CI PPR Behavior)	ppr.ci.beh.errmessage.list	string	0 or 1	0: normal split completion transaction 1: split completion error message
DELAY List (CI PPR Behavior)	ppr.ci.beh.delay.list	string	1 ... 65535	List of numbers of clock delays before REQ# is asserted
STEPS List (CI PPR Behavior)	ppr.ci.beh.steps.list	string	2 ... 6	List of numbers of address steps
REQ64 List (CI PPR Behavior)	ppr.ci.beh.req64.list	string	0, 1	1: 64-bit data transfer 0: No 64-bit data transfer access

Card Property used in the GUI	Card Property used in the Settings File	Type	Range	Description
RELREQ List (CI PPR Behavior)	ppr.ci.beh.relreq.list	string	1 ... 2047	List of number of cycles after which REQ# is released after assertion of FRAME#
DECSPEED List (CT PPR Behavior)	ppr.ct.beh.decspeed.list	string	A, B, C	List of decode speeds
ACK64 List (CT PPR Behavior)	ppr.ct.beh.ack64.list	string	No, Yes	List that determine s whether a 64-bit data transfer acknowledge will be asserted or will not be asserted
INITIAL List (CT PPR Behavior)	ppr.ct.beh.initial.list	string	Accept Single Retry TAbort	List that determines the initial behavior of the completer-target response
LATENCY List (CT PPR Behavior)	ppr.ct.beh.latency.list	string	3 ... 34	List of numbers of initial latency clocks
SUBSEQ List (CT PPR Behavior)	ppr.ct.beh.subseq.list = "Accept,Disconnect"	string	Accept Disconnect	List that specifies the target response in subsequent data phases. 0: accepts all subsequent data phases 1: disconnects in the selected data phase
SUBSECPHASE List (CT PPR Behavior)	ppr.ct.beh.subseqphase.list	string	0 ... 2047	List of selected subsequent data phases
SPLITLATENCY List (CT PPR Behavior)	ppr.ct.beh.splitlatency.list	string	3 ... 18	List of numbers of wait cycles. A split response is signaled after the specified number of wait cycles.
SPLITENABLE List (CT PPR Behavior)	ppr.ct.beh.splitenable.list	string	0 or 1	0: No split response will be generated 1: A split response will be generated

Protocol Checker (Rule Masking)

Card Property used in the GUI	Testcard Property used in the Settings File	Type	Range	Description
Protocol Rule Masking State Disabled (lower bits)	protocolrule.mask.lo	DWORD	32	Masked protocol rules (bit 0 ... 31).
Protocol Rule Masking State Disabled (higher bits)	protocolrule.mask.hi	DWORD	20	Masked protocol rules (bit 32 ... 51).
Mask Rule(s) After x Occurrences	protocolrule.mask.count	DWORD	0 ... (2 ³² - 1)	Number of occurrences the rule is masked.

Index

A

automatic rule masking 67
available tests
 overview 44

B

basic test structure 43

C

card features
 properties (GUI) 81
card number LEDs 41
card numbers
 identification 40
common protocol errors 75
completer
 PCI-X testcard properties (GUI) 86
coverage of the tests 10

D

duration 64
 estimation 68

E

error types 70
errors
 data compare errors 74
 during test run 75
 during the test function 74
 handling 74
 in the protocol 75
 master abort condition 74
 on the testcard 74
 PCI protocol errors 74
 PPR errors 75
 testcards detection errors 74
estimating test durations 68
example
 setting file formats 78
external control 38

F

features
 testcard 67
formats
 settings file 78
Front Side Interface Executable 39
FSI-E 39
FSI-Executable 39

H

hardware configurations 37

I

insert new tests 63
internal control 38

L

LEDs on the testcard 40
log file
 contents 72
 description 72
 view 72

M

master
 PCI testcard properties (GUI) 82

O

only System Validation Package traffic 57
overview of available tests 44

P

PCI testcard settings (GUI)
 master 82
PCISIG Compliance Tests 51
PCI-X testcard settings (GUI)
 completer 86
 requester 85
performance of the testcard 70
permutation of the PCI protocols 11
power LED 40
PPR report files 73
PPR technology 11
predefined tests 63
principles of testing 60
properties (GUI)
 card features 81
protocol
 attributes tested 11
 errors 75
protocol checker 67
 testcard properties (GUI) 87

R

recommended configuration 38
remove available tests 65
report files
 contents 73
 description 73
requester
 PCI-X testcard properties (GUI) 85
requirements for scenarios 61
results
 testing 71
rule masking
 automatic 67

S

scenario requirements 61
selecting testcards 65
selecting tests 62
setting file formats
 example 78
settings
 testcard 66
settings file
 formats 78
start
 test 69
start delay 64
static report 69
SVP software
 application 7
 features 7
system stress test
 recommended duration 57

T

target
 testcard properties (GUI) 84
test
 descriptions 43
 predefined tests 63
 principles 60
 repeatability 7
 run 69
 start 69
 structure 43
test configuration
 overview 61
test duration
 estimation 68

- test function
 - errors 74
- test results 71
- testcard
 - cross triggering 68
 - errors 74
 - external triggering 68
 - performance 70
 - performance measurement 67
 - protocol checker 67
 - settings 66
 - trace memory 67
- testcard control 38
- testcard features 67
- testcard information
 - properties (GUI) 80
- testcard location
 - properties (GUI) 80
- testcard settings (GUI)
 - protocol checker 87
 - target 84
 - testcard features 81
 - testcard information 80
 - testcard location 80
- testing time 64
- tests provided by the Agilent 2976A
 - busload generator 45
 - CPU and testcard to system memory 47
 - CPU to testcard 46
 - CPU to testcard address and testcard to system memory address 54
 - CPU to testcard I/O space 47
 - CPU to testcard memory space 47
 - DISCARD - discard test 56
 - master-to-target traffic 49
 - MCT Test - maximum completion time test 56
 - MLT - master latency test 51
 - MTEST - power management test 55
 - PCI configuration scan 50
 - peer-to-peer traffic 48
 - protocol checker 50
 - SIG card test 55
 - SIG interrupt routing test 53
 - SIG post test 52
 - testcard read from system memory 50
 - testcard to system memory 46
 - testcard to system memory - user address 51
 - TYPE1 - type 1 test 56
- total duration 64
- traffic caused by multiple devices 57
- trigger out line 68
- triggering
 - cross 68
 - external 68

V

- view test settings 63
- violation of protocol rules 75